RJ6 Block Diagram

1

CPU
Yonah/Merom
478 PIN (micro FC-PGA)
P3,4

FSB 667 MHz(166X4)

14.318MHz

CLOCK GEN
ICS954310
P 2

DVI

M56
P36-40

LVDS
LCD P7
LVDS

R/G/B
CRT P11
R/G/B

PCIE 16Lanes

Calistoga
945GM/PM
1466 PIN (micro FCBGA)
37.5mm x 37.5mm
P5-10

DDRII 400/533/667
UNBUFFERED DDRII SODIMM P12

DDRII 400/533/667
UNBUFFERED DDRII SODIMM P12

DMI(2X, 4X)

RJ45 (Giga)
LAN
MARVELL 88E8055
P27

PCIE

PCI-E Mini
Intel 3945
P19

PCIE

ICH7-M
652 BGA
31mm x 31mm
P13-16

Azalia Link

ALC260
P22

MDC Module
P19

TI-TPA6011A4
P23

RJ11

MIC. Jack
Audio Jack
INT.SPKR.

PCI BUS

USB 1.1/2.0

USB 1.1/2.0

SATA

3.3V LPC,33MHZ

TPM 1.2 Sinosun SSX35ACB
P25

HDD
P24

USB
VT6212
P35

TI_7411
P17-18

SATA
Sil 3512
P34

USB*3
P26

BAY P24

Docking*3 P25

Finger Print P26

PCU
NS PC87541
P21

Felica P24
Blue Tooth P24
Camera P26
WWAN P24

PCMCIA P20

1394 P17

Memory Stick Pro(DUO)
SD/MMC
P18

Doacking P25

BAY P24

TOUCH PAD
T/P SWITCH

INT.K/B P26
Track Point

BIOS P21

Camera LED
HDD LED
Wireless SW
Wireless LED
Bluetooth SW
Bluetooth LED
LED Power/Speep/Bat/HDD

ADI
ADXL322JCP
P24

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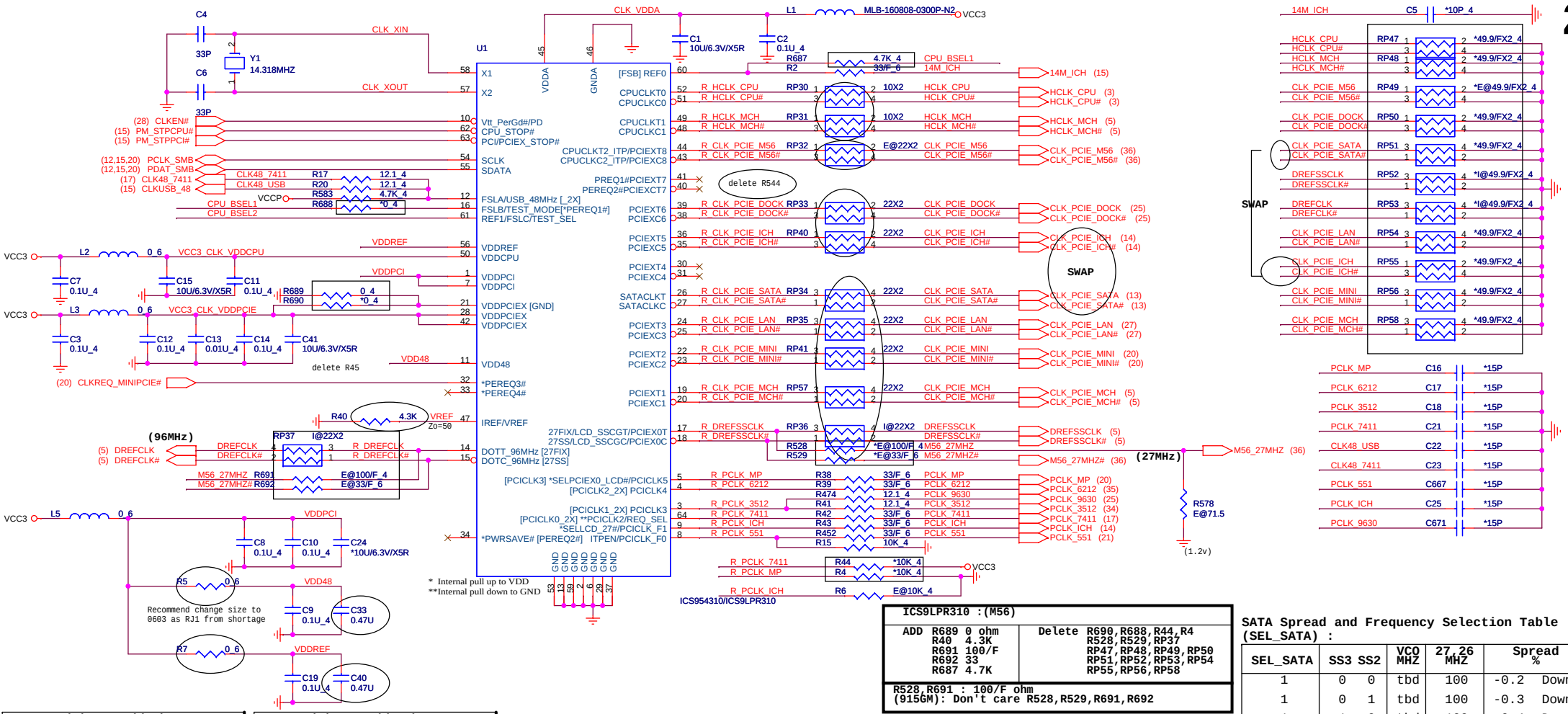
QUANTA COMPUTER

Size	Document Number	Rev
	RJ6 Main Board	1A
Date: Tuesday, April 11, 2006	Sheet 1 of 40	



ICS9LPR310 :(M56)

ADD R689 0 ohm R40 4.3K R691 100/F R692 33 R687 4.7K	Delete R690,R688,R44,R4 R528,R529,RP37 RP47,RP48,RP49,RP50 RP51,RP52,RP53,RP54 RP55,RP56,RP58

R528,R691 : 100/F ohm
(915GM): Don't care R528,R529,R691,R692

SEL_SRC0(Pin 17,18)(R4)

0: LCDCLK Pair
1: SRCCLK0 pair

REQ_SEL(Pin 40,41)(R44)

0: PCIEXT7/PCIEXC7
1: PREQ#

SEL_LCD(Pin 17,18)(R6)

0: 27MHZSS/27MHZSS# pair (M56)
1: LCDCLK pair (945GM)

IREF (Pin 39) :

475_1% : Sets the IREF current to 2.32mA

SATA Spread and Frequency Selection Table (SEL_SATA) :

SEL_SATA	SS3	SS2	VCO MHZ	27_26 MHZ	Spread %	
1	0	0	tbd	100	-0.2	Down
1	0	1	tbd	100	-0.3	Down
1	1	0	tbd	100	-0.4	Down
1	1	1	tbd	100	-0.5	Down

LCDCLK Spread and Frequency Selection Table (SEL_LCD) :

SEL_LCD	SS3	SS2	SS1	SS0	17,18 MHZ	Spread %		SEL_LCD	SS3	SS2	SS1	SS0	17,18 MHZ	Spread %	
1	0	0	0	0	96	+/-1.5		0	0	0	0	0	27	+/-0.25	
1	0	0	0	1	96	+/-1.25		0	0	0	0	1	27	+/-0.5	
1	0	0	1	0	96	+/-1.0		0	0	0	1	0	27	+/-0.75	
1	0	0	1	1	96	+/-0.8	Center	0	0	0	1	1	27	+/-1	Center
1	0	1	0	0	96	+/-0.6		0	0	1	0	0	27	+/-1.25	
1	0	1	0	1	96	+/-0.5		0	0	1	0	1	27	+/-1.5	
1	0	1	1	0	96	+/-0.4		0	0	1	1	0	27	+/-1.75	
1	0	1	1	1	96	+/-0.3		0	0	1	1	1	27	+/-2	
1	1	0	0	0	96	3		0	1	0	0	0	27	-0.5	
1	1	0	0	1	96	2.5		0	1	0	0	1	27	-1	
1	1	0	1	0	96	2		0	1	0	1	0	27	-1.25	
1	1	0	1	1	96	1.75	Down	0	1	0	1	1	27	-1.5	Down
1	1	1	0	0	96	1.5		0	1	1	0	0	27	-1.75	
1	1	1	0	1	96	1.25		0	1	1	0	1	27	-2	
1	1	1	1	0	96	1		0	1	1	1	0	27	-2.5	
1	1	1	1	1	96	0.8		0	1	1	1	1	27	-3	

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %	
0	0	0	266.66	100	33.33	14.318	48	96	0.5	Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5	Down
0	1	0	200.00	100	33.33	14.318	48	96	0.5	Down
* 0	1	1	166.66	100	33.33	14.318	48	96	0.5	Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5	Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5	Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5	Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5	Down

Signal		945GM	945PM
	R578	NI	71.5
CLK_PCIE_M56	RP32	NI	33X2
	RP49	NI	49.9
DREFSSCLK	RP36	33X2	NI
	RP52	49.9X2	NI
	R528	NI	121
	R529	NI	33
DREFCLK	RP37	33X2	NI
	RP53	49.9X2	NI
R_PCLK_ICH	R6	NI	10K

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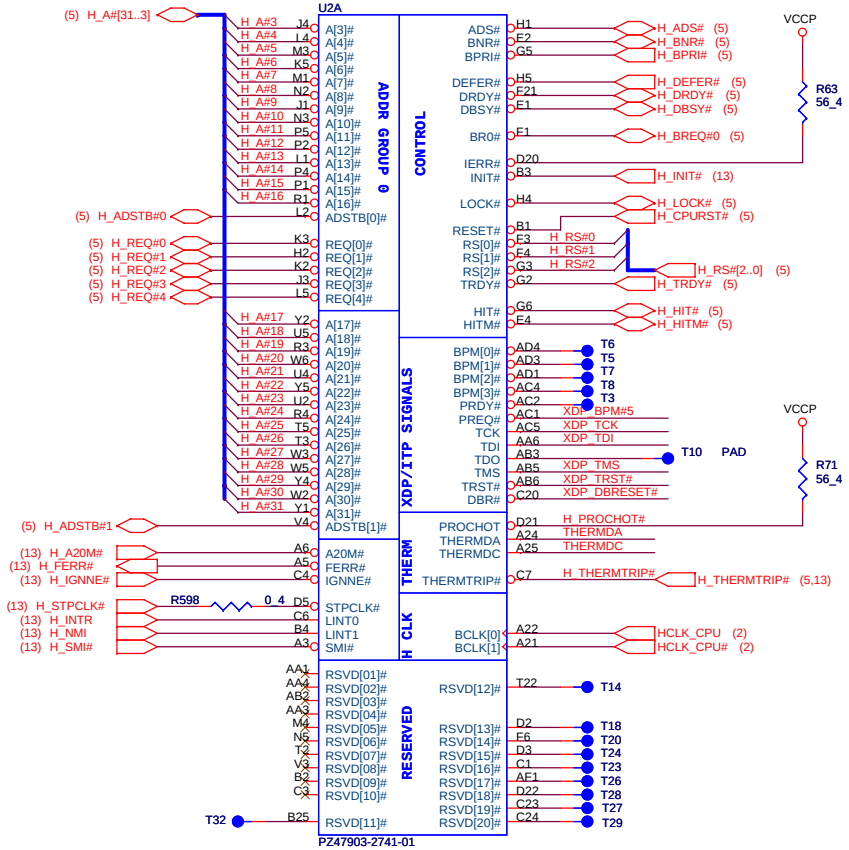
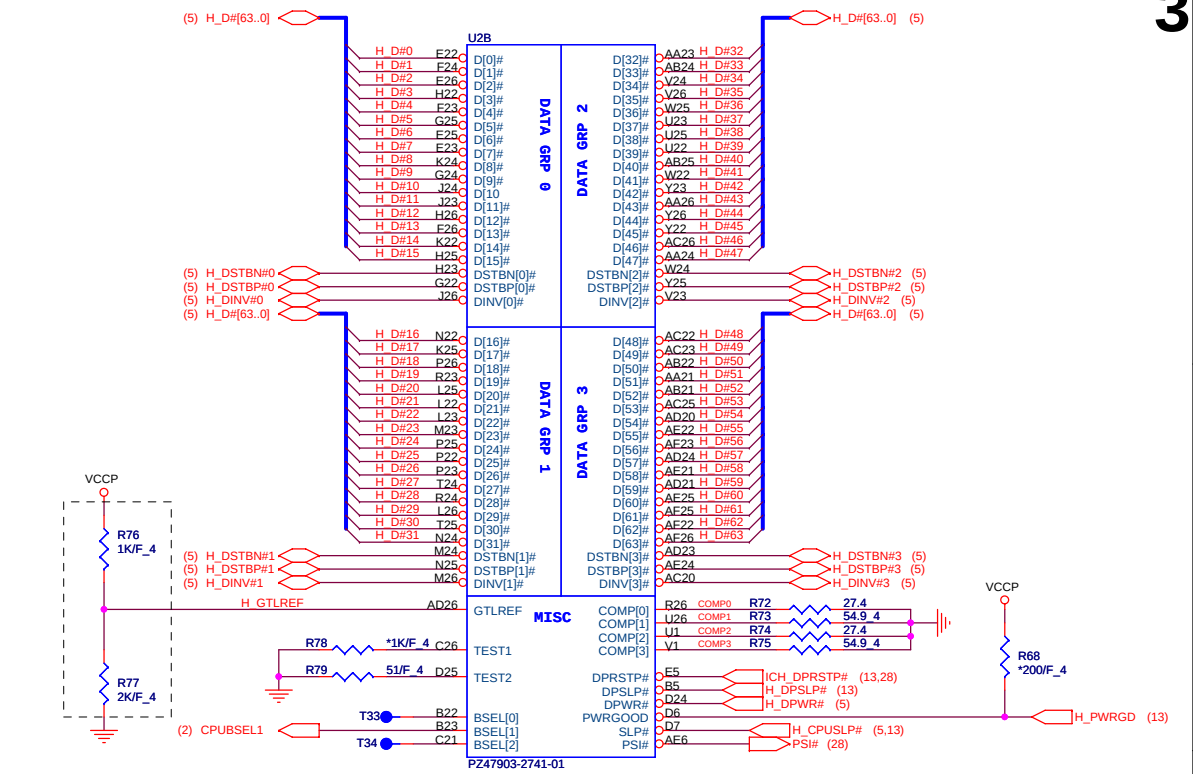
QUANTA COMPUTER

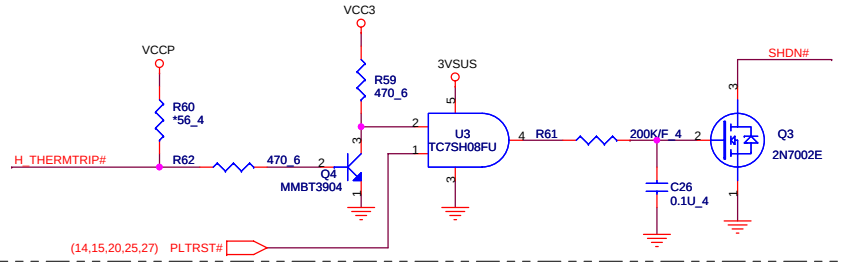
Title: CLOCK GENERATOR

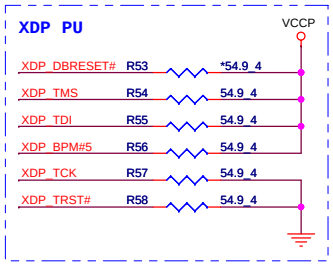
Size: Custom | Document Number: RJ6 Main Board | Rev: 2A

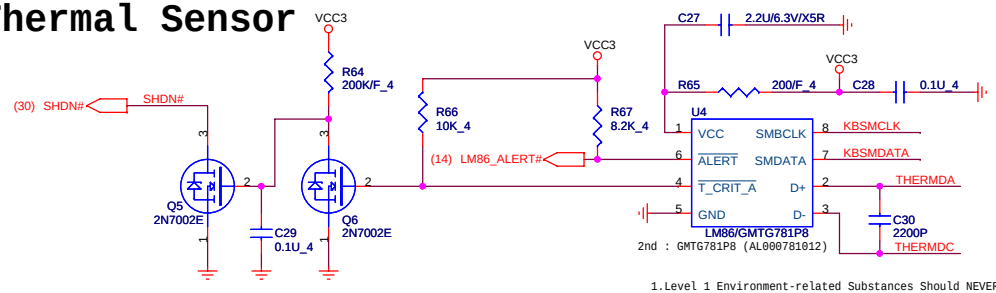
Date: Wednesday, May 03, 2006 | Sheet 2 of 40

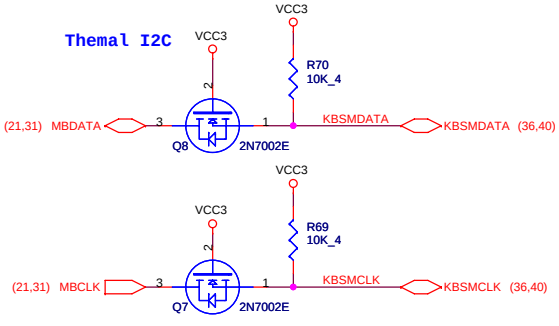


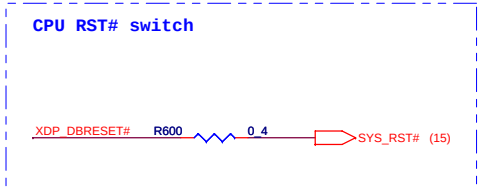












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QUANTA COMPUTER

Title	CPU1 of 2	
Size	Document Number: RJ6 Main Board	Rev: 1B
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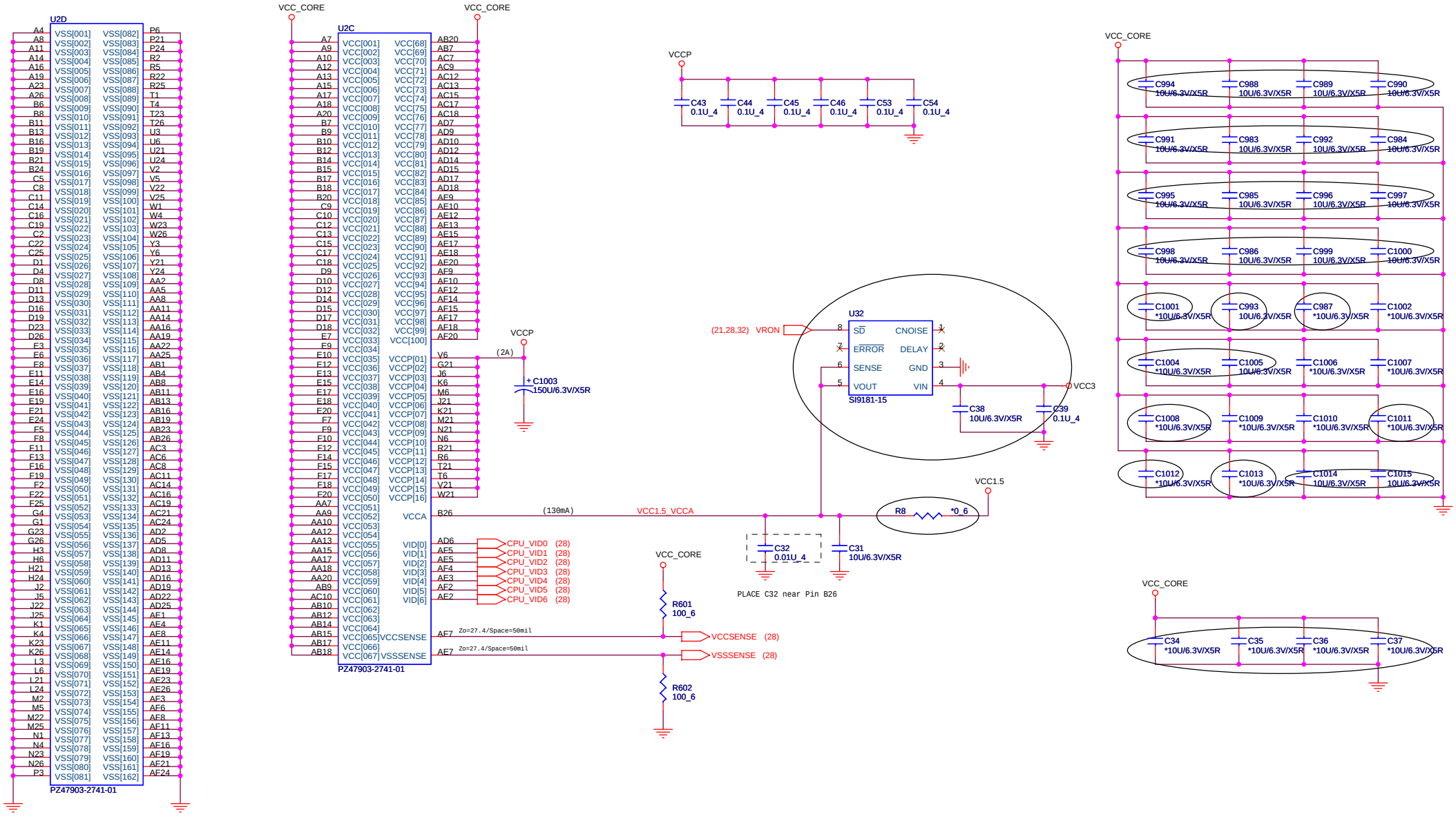

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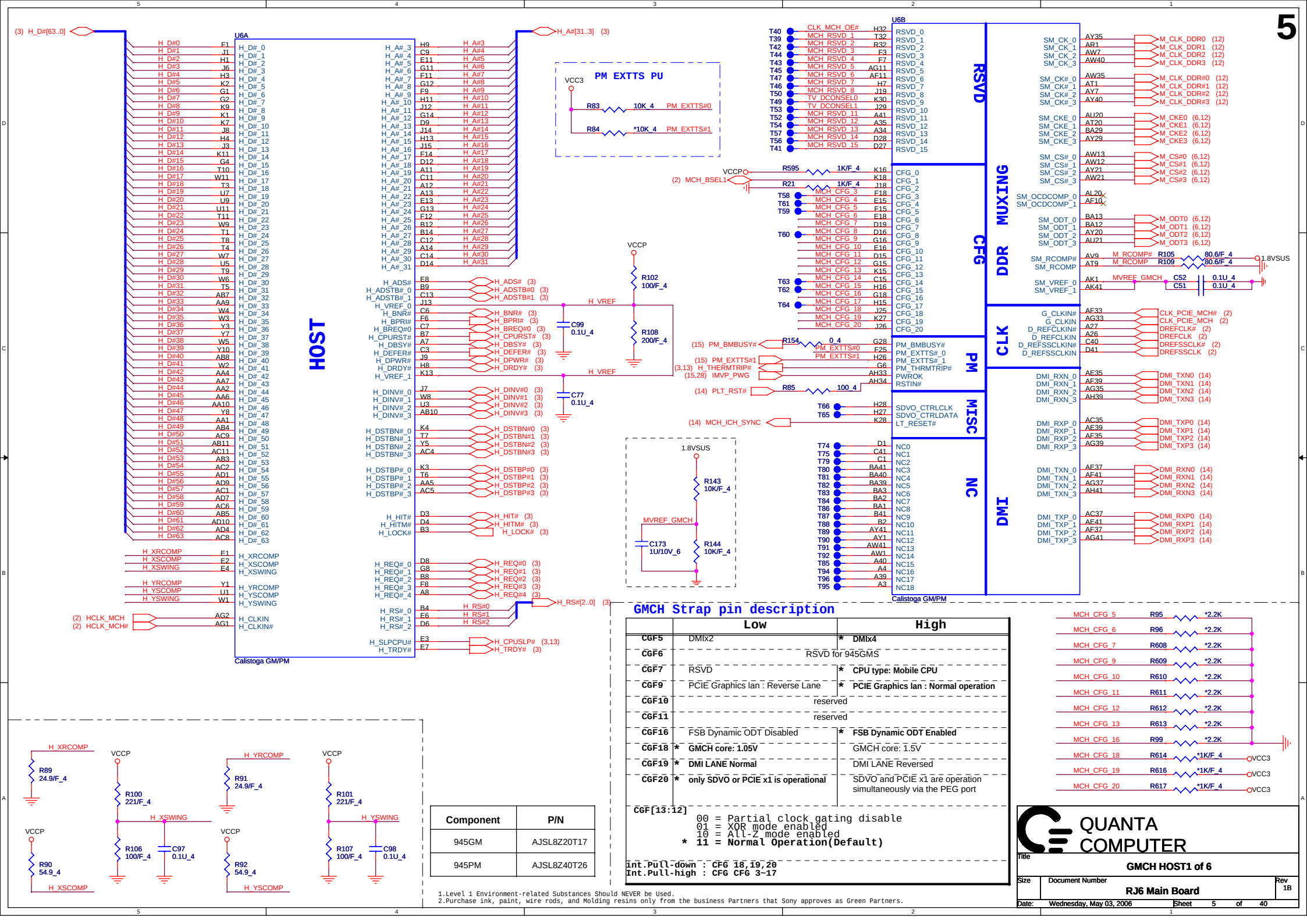
QUANTA COMPUTER

Title	CPU 2 of 2	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Wednesday, May 03, 2006	Sheet 4 of 40	



GMCH Strap pin description

	Low	High
CGF5	DMIx2	* DMIx4
CGF6	RSVD for 945GMS	
CGF7	RSVD	* CPU type: Mobile CPU
CGF9	PCIE Graphics lan : Reverse Lane	* PCIE Graphics lan : Normal operation
CGF10	reserved	
CGF11	reserved	
CGF16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
CGF18	* GMCH core: 1.05V	GMCH core: 1.5V
CGF19	* DMI LANE Normal	DMI LANE Reversed
CGF20	* only SDVO or PCIE x1 is operational	SDVO and PCIE x1 are operation simultaneously via the PEG port

CGF[13:12]

00 = Partial clock gating disable
01 = XOR mode enabled
10 = All-Z mode enabled
* 11 = Normal Operation(Default)

int.Pull-down : CFG 18,19,20
int.Pull-high : CFG CFG 3~17

Component	P/N
945GM	AJSL8Z20T17
945PM	AJSL8Z40T26

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QUANTA COMPUTER

Title	GMCH HOST1 of 6	
Size	Document Number: RJ6 Main Board	Rev: 1B
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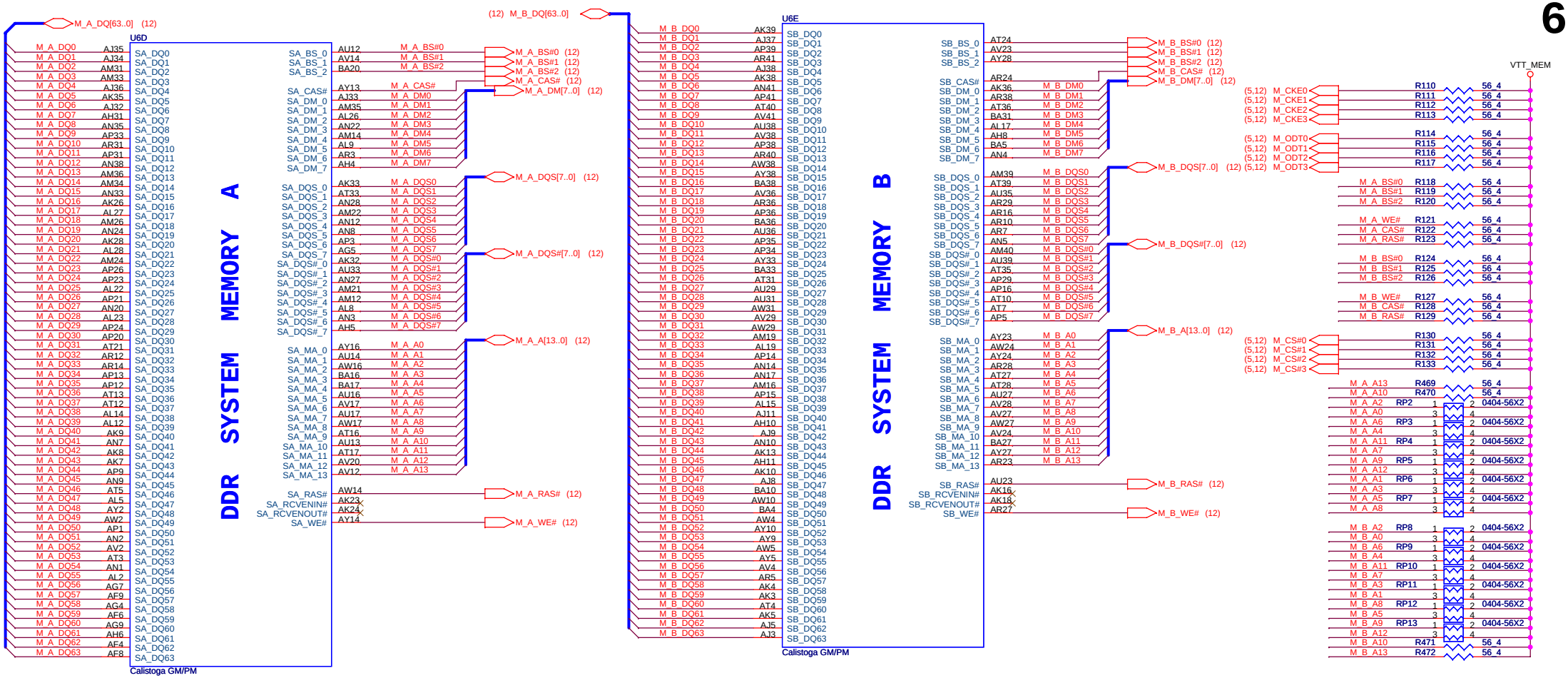

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QUANTA COMPUTER

Title	GMCH DDR II 2 of 6	
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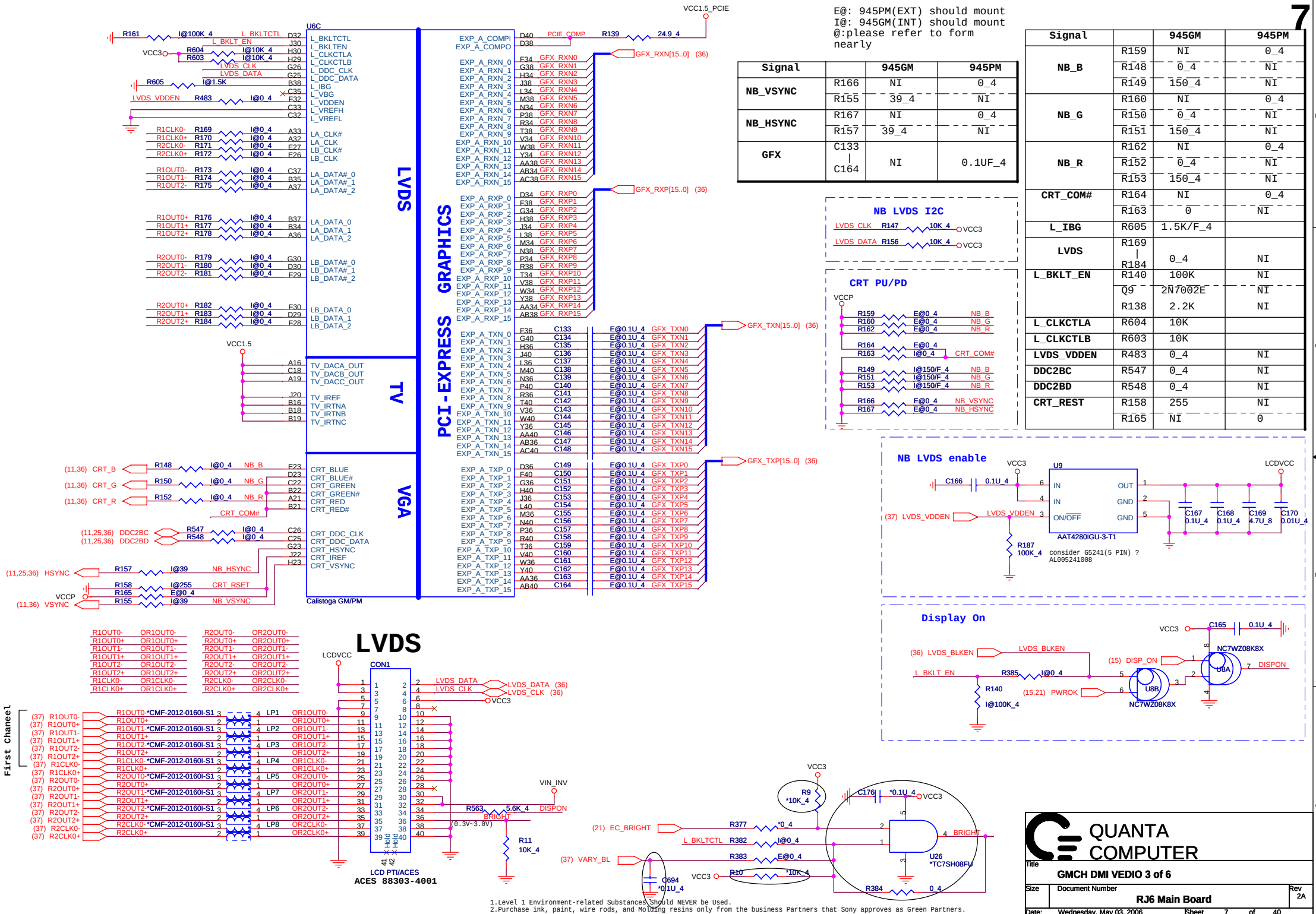
E@: 945PM(EXT) should mount
I@: 945GM(INT) should mount
@:please refer to form nearly

Signal		945GM	945PM
NB_VSYNC	R166	NI	0_4
	R155	39_4	NI
NB_HSYNC	R167	NI	0_4
	R157	39_4	NI
GFX	C133 | C164	NI	0.1UF_4

Signal		945GM	945PM
NB_B	R159	NI	0_4
	R148	0_4	NI
	R149	150_4	NI
NB_G	R160	NI	0_4
	R150	0_4	NI
	R151	150_4	NI
NB_R	R162	NI	0_4
	R152	0_4	NI
	R153	150_4	NI
CRT_COM#	R164	NI	0_4
	R163	0	NI
L_IBG	R605	1.5K/F_4	
LVDS	R169 | R184	0_4	NI
L_BKLT_EN	R140	100K	NI
	Q9	2N7002E	NI
	R138	2.2K	NI
L_CLKCTLA	R604	10K	
L_CLKCTLB	R603	10K	
LVDS_VDDEN	R483	0_4	NI
DDC2BC	R547	0_4	NI
DDC2BD	R548	0_4	NI
CRT_REST	R158	255	NI
	R165	NI	0



Title	GMCH DMI VEDIO 3 of 6
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U6G

VCCP

C1016 220U

(915GM 5.5A)
(915PM 1.5A)

VCC_0 VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75 VCC_76 VCC_77 VCC_78 VCC_79 VCC_80 VCC_81 VCC_82 VCC_83 VCC_84 VCC_85 VCC_86 VCC_87 VCC_88 VCC_89 VCC_90 VCC_91 VCC_92 VCC_93 VCC_94 VCC_95 VCC_96 VCC_97 VCC_98 VCC_99 VCC_100 VCC_101 VCC_102 VCC_103 VCC_104 VCC_105 VCC_106 VCC_107 VCC_108 VCC_109 VCC_110

VCC

VCC_SM_0 VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35 VCC_SM_36 VCC_SM_37 VCC_SM_38 VCC_SM_39 VCC_SM_40 VCC_SM_41 VCC_SM_42 VCC_SM_43 VCC_SM_44 VCC_SM_45 VCC_SM_46 VCC_SM_47 VCC_SM_48 VCC_SM_49 VCC_SM_50 VCC_SM_51 VCC_SM_52 VCC_SM_53 VCC_SM_54 VCC_SM_55 VCC_SM_56 VCC_SM_57 VCC_SM_58 VCC_SM_59 VCC_SM_60 VCC_SM_61 VCC_SM_62 VCC_SM_63 VCC_SM_64 VCC_SM_65 VCC_SM_66 VCC_SM_67 VCC_SM_68 VCC_SM_69 VCC_SM_70 VCC_SM_71 VCC_SM_72 VCC_SM_73 VCC_SM_74 VCC_SM_75 VCC_SM_76 VCC_SM_77 VCC_SM_78 VCC_SM_79 VCC_SM_80 VCC_SM_81 VCC_SM_82 VCC_SM_83 VCC_SM_84 VCC_SM_85 VCC_SM_86 VCC_SM_87 VCC_SM_88 VCC_SM_89 VCC_SM_90 VCC_SM_91 VCC_SM_92 VCC_SM_93 VCC_SM_94 VCC_SM_95 VCC_SM_96 VCC_SM_97 VCC_SM_98 VCC_SM_99 VCC_SM_100 VCC_SM_101 VCC_SM_102 VCC_SM_103 VCC_SM_104 VCC_SM_105 VCC_SM_106 VCC_SM_107

Calistoga GM/PM

VCCSM_LF4 VCCSM_LF5

C1017 0.47U
C1025 0.47U

667MHz: 3.2A
533MHz : 2.8A
400MHz : 2.4A

1.8VSUS

C1023 *330U
C1024 4.7U
C1028 4.7U
C1029 0.1U_4
C1030 0.1U_4
C1031 0.1U_4
C1032 0.1U_4
C1040 0.1U_4
C1101 *330U
C1102 330U

C1033 0.47U
C1034 0.47U
place C50 on BA23 Ball
place C49 on AJ23 Ball

C172 0.47U
place C51 on BA15 Ball

VCCSM_LF2 VCCSM_LF1

C1036 0.47U
C1035 0.47U

VCCP

C1018 220U
C1019 4.7U
C1026 4.7U
C1021 0.1U_4
C1022 0.1U_4
C1027 0.1U_4

U6F

VCC_NCTF0 VCC_NCTF1 VCC_NCTF2 VCC_NCTF3 VCC_NCTF4 VCC_NCTF5 VCC_NCTF6 VCC_NCTF7 VCC_NCTF8 VCC_NCTF9 VCC_NCTF10 VCC_NCTF11 VCC_NCTF12 VCC_NCTF13 VCC_NCTF14 VCC_NCTF15 VCC_NCTF16 VCC_NCTF17 VCC_NCTF18 VCC_NCTF19 VCC_NCTF20 VCC_NCTF21 VCC_NCTF22 VCC_NCTF23 VCC_NCTF24 VCC_NCTF25 VCC_NCTF26 VCC_NCTF27 VCC_NCTF28 VCC_NCTF29 VCC_NCTF30 VCC_NCTF31 VCC_NCTF32 VCC_NCTF33 VCC_NCTF34 VCC_NCTF35 VCC_NCTF36 VCC_NCTF37 VCC_NCTF38 VCC_NCTF39 VCC_NCTF40 VCC_NCTF41 VCC_NCTF42 VCC_NCTF43 VCC_NCTF44 VCC_NCTF45 VCC_NCTF46 VCC_NCTF47 VCC_NCTF48 VCC_NCTF49 VCC_NCTF50 VCC_NCTF51 VCC_NCTF52 VCC_NCTF53 VCC_NCTF54 VCC_NCTF55 VCC_NCTF56 VCC_NCTF57 VCC_NCTF58 VCC_NCTF59 VCC_NCTF60 VCC_NCTF61 VCC_NCTF62 VCC_NCTF63 VCC_NCTF64 VCC_NCTF65 VCC_NCTF66 VCC_NCTF67 VCC_NCTF68 VCC_NCTF69 VCC_NCTF70 VCC_NCTF71 VCC_NCTF72

NCTF

VSS_NCTF0 VSS_NCTF1 VSS_NCTF2 VSS_NCTF3 VSS_NCTF4 VSS_NCTF5 VSS_NCTF6 VSS_NCTF7 VSS_NCTF8 VSS_NCTF9 VSS_NCTF10 VSS_NCTF11 VSS_NCTF12

VCCAUX_NCTF0 VCCAUX_NCTF1 VCCAUX_NCTF2 VCCAUX_NCTF3 VCCAUX_NCTF4 VCCAUX_NCTF5 VCCAUX_NCTF6 VCCAUX_NCTF7 VCCAUX_NCTF8 VCCAUX_NCTF9 VCCAUX_NCTF10 VCCAUX_NCTF11 VCCAUX_NCTF12 VCCAUX_NCTF13 VCCAUX_NCTF14 VCCAUX_NCTF15 VCCAUX_NCTF16 VCCAUX_NCTF17 VCCAUX_NCTF18 VCCAUX_NCTF19 VCCAUX_NCTF20 VCCAUX_NCTF21 VCCAUX_NCTF22 VCCAUX_NCTF23 VCCAUX_NCTF24 VCCAUX_NCTF25 VCCAUX_NCTF26 VCCAUX_NCTF27 VCCAUX_NCTF28 VCCAUX_NCTF29 VCCAUX_NCTF30 VCCAUX_NCTF31 VCCAUX_NCTF32 VCCAUX_NCTF33 VCCAUX_NCTF34 VCCAUX_NCTF35 VCCAUX_NCTF36 VCCAUX_NCTF37 VCCAUX_NCTF38 VCCAUX_NCTF39 VCCAUX_NCTF40 VCCAUX_NCTF41 VCCAUX_NCTF42 VCCAUX_NCTF43 VCCAUX_NCTF44 VCCAUX_NCTF45 VCCAUX_NCTF46 VCCAUX_NCTF47 VCCAUX_NCTF48 VCCAUX_NCTF49 VCCAUX_NCTF50 VCCAUX_NCTF51 VCCAUX_NCTF52 VCCAUX_NCTF53 VCCAUX_NCTF54 VCCAUX_NCTF55 VCCAUX_NCTF56 VCCAUX_NCTF57

VCC1.5

Calistoga GM/PM

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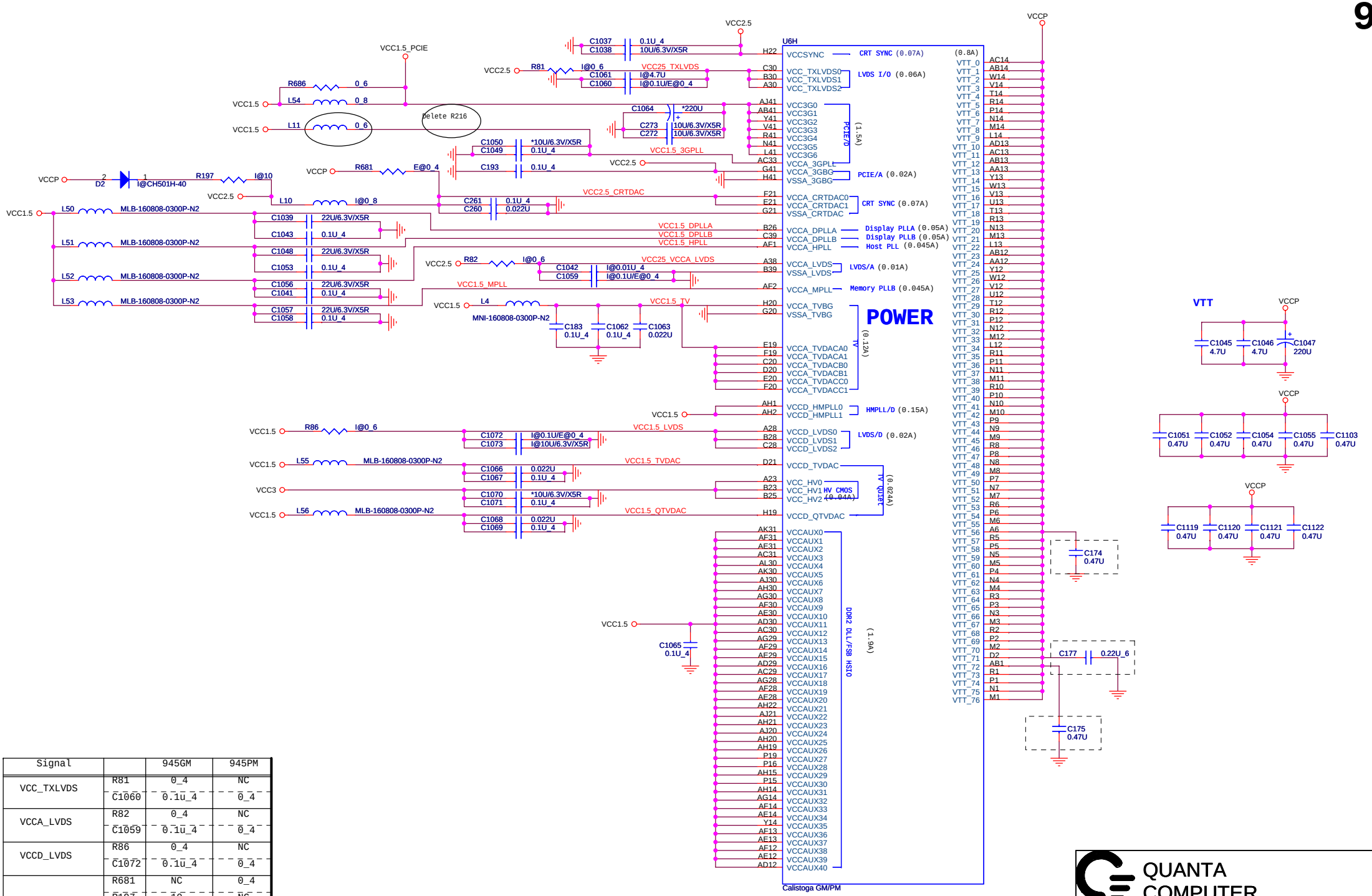
QUANTA COMPUTER

Title	GMCH Power & Strap 4 of 6	
Size	Document Number: RJ6 Main Board	Rev: 1A
Date: Wednesday, May 03, 2006	Sheet 8 of 40	



Signal		945GM	945PM
VCC_TXLVDS	R81	0_4	NC
	C1060	0.1u_4	0_4
VCCA_LVDS	R82	0_4	NC
	C1059	0.1u_4	0_4
VCCD_LVDS	R86	0_4	NC
	C1072	0.1u_4	0_4
VCC2.5_CRTDAC	R681	NC	0_4
	R197	10	NC
	L10	MNI-160808-0300P-N2	NC
	D2	CH501H-40	NC

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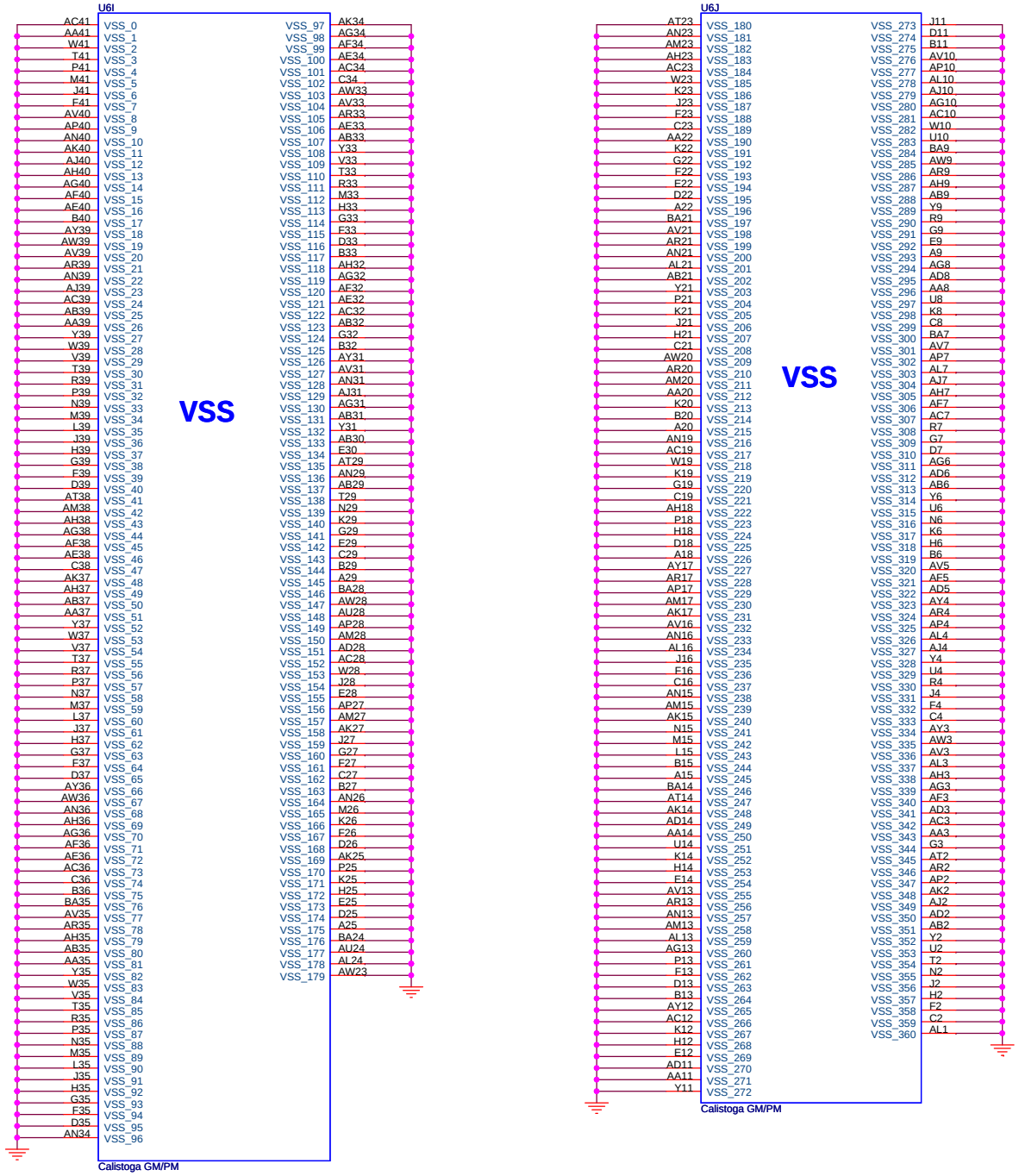
QUANTA COMPUTER

Title	GMCH Power 2 5 of 6	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Wednesday, May 03, 2006	Sheet 9 of 40	



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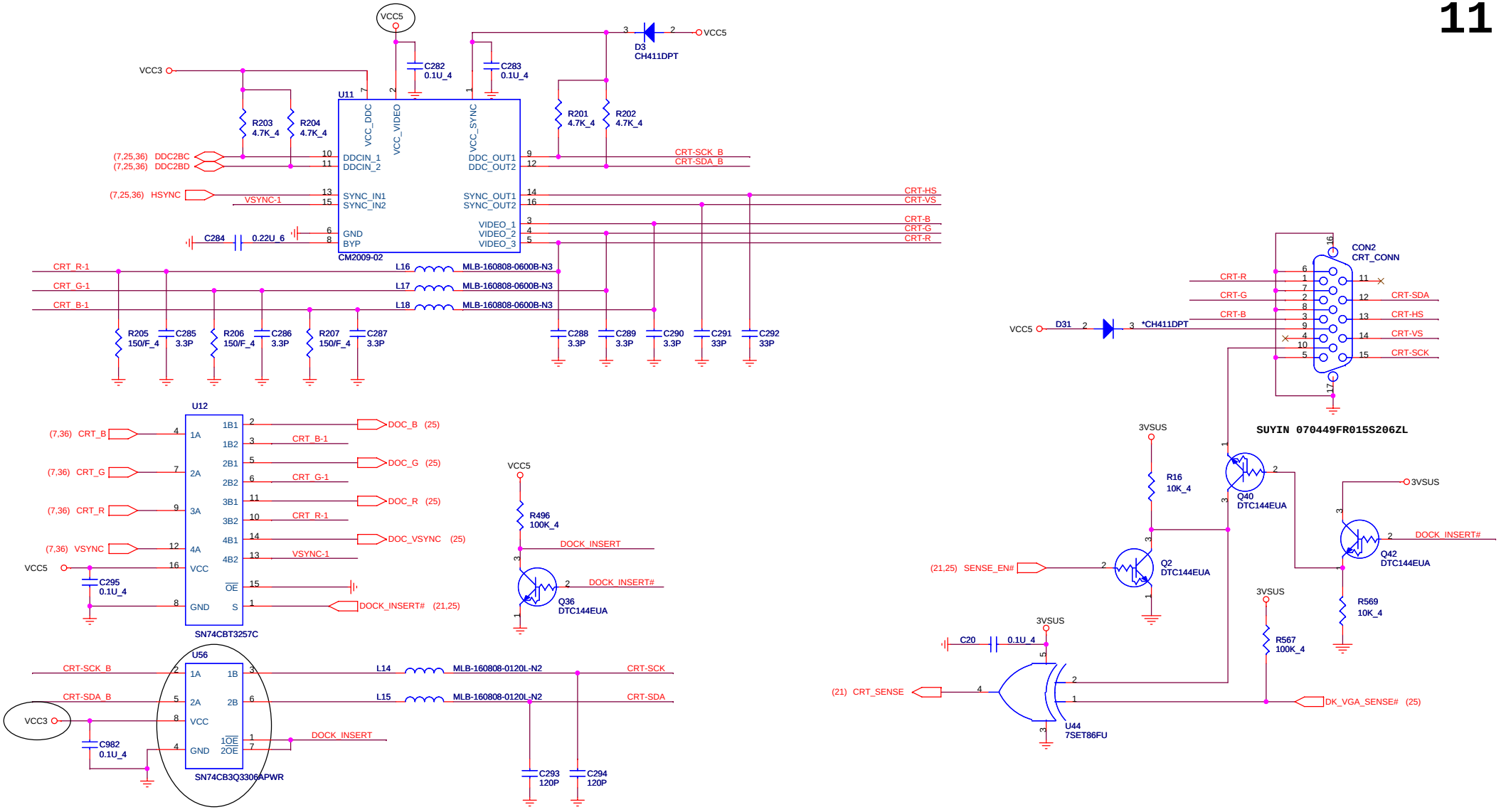
QUANTA COMPUTER

Title	GMCH GND 6 of 6	
Size	Document Number: RJ6 Main Board	Rev: 1A
Date: Wednesday, May 03, 2006	Sheet 10 of 40	



SN74CBT3257

OE	S	1A
H	H	L
H	L	H
L	H	H
L	L	L

	SENSE_EN#	MB CRT	DOCK CRT	DOCK DVI	CRT_SENSE
All no Plug	L	H	H	L	L
MB CRT Plug	L	L	H	L	H
DOCK CRT Plug	L	H	L	L	H
DOCK DVI Plug	L	H	H	H	H
SENSE EN	H	X	X	X	L
DOCK CRT/DVI Plug	L	H	L	H	L
DOCK CRT/MB CRT Plug	L	L	L	L	L

1.Level 1 Environment-related Substances Should NEVER be Used.
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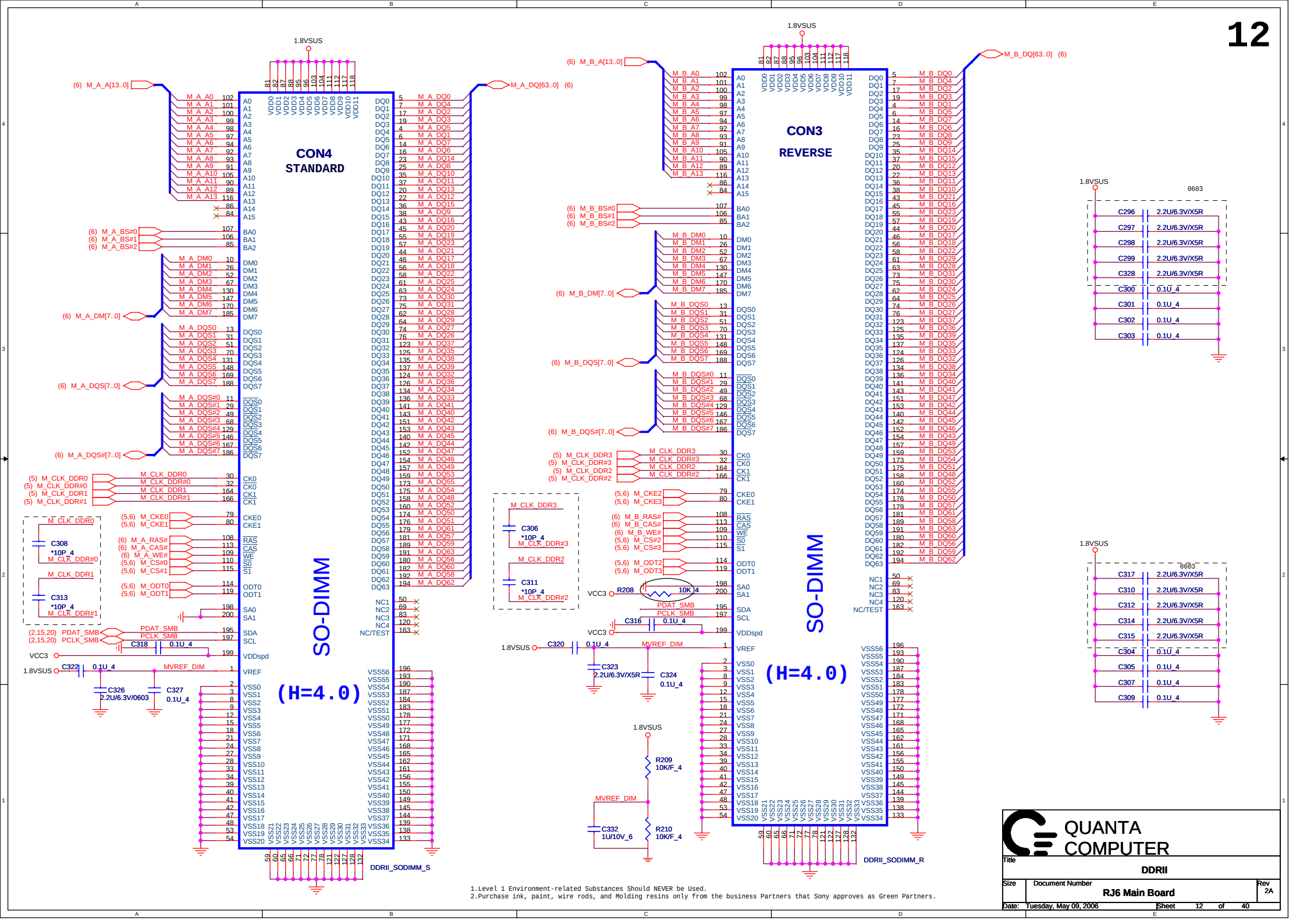
QUANTA COMPUTER

Title	CRT	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Wednesday, May 03, 2006	Sheet 11 of 40	

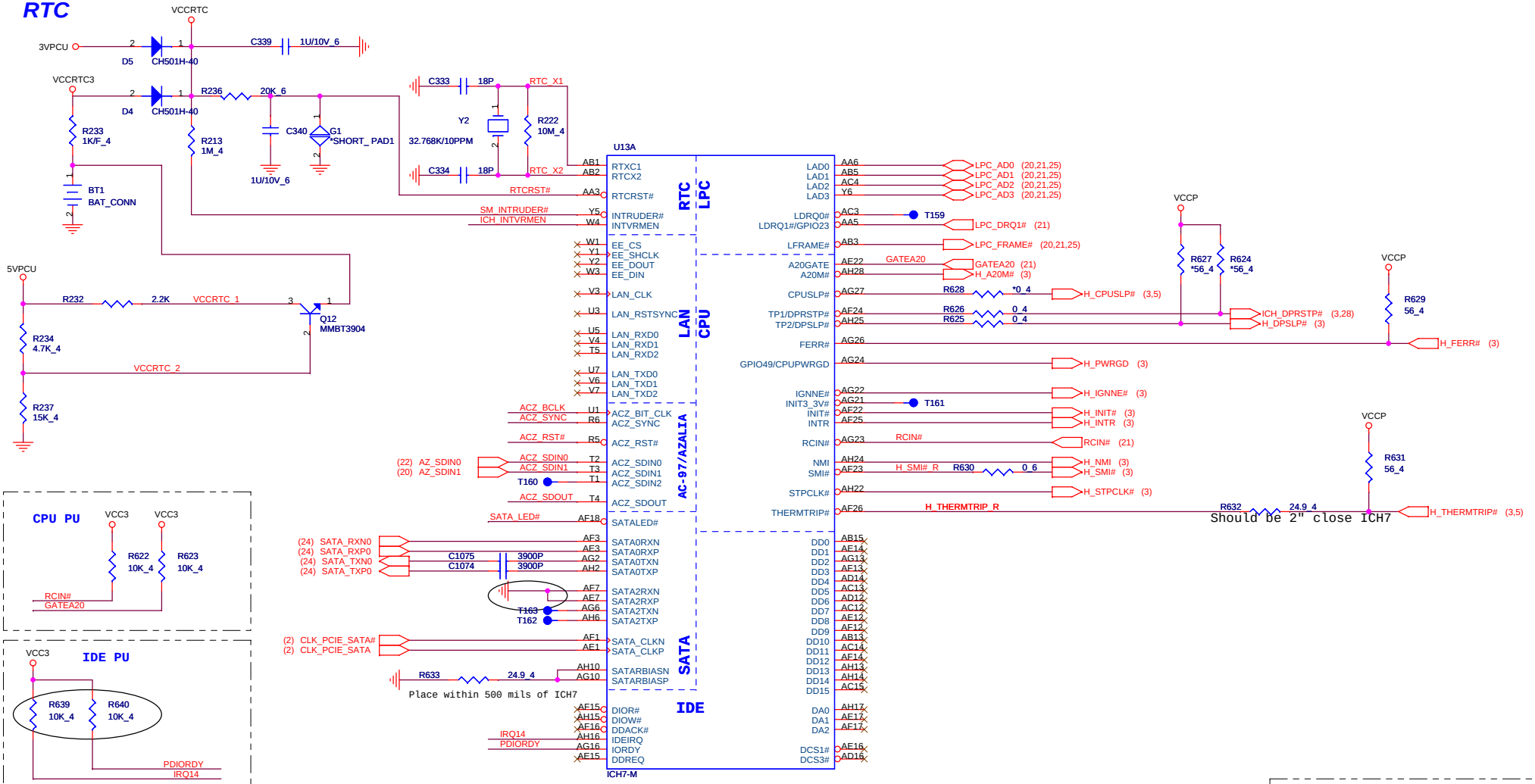


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

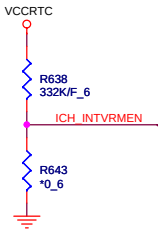
QUANTA COMPUTER

Title	DDRII	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Tuesday, May 09, 2006	Sheet 12 of 40	

RTC

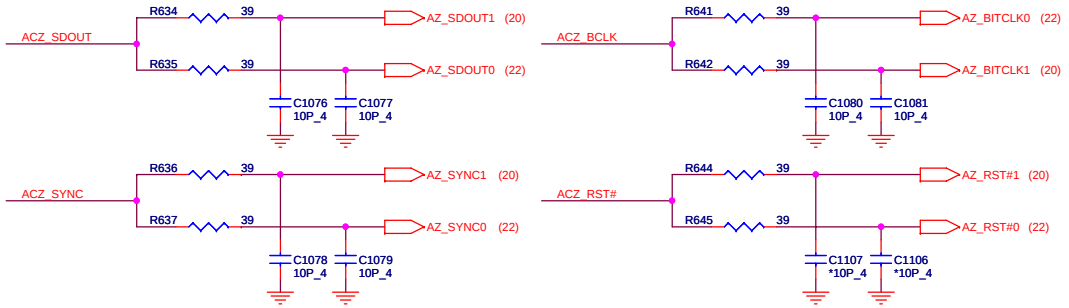


ICH7 internal VR enable strap



	INTVRMEN
Enable (default)	1
Disable	0

HD Audio to Codec and Modem



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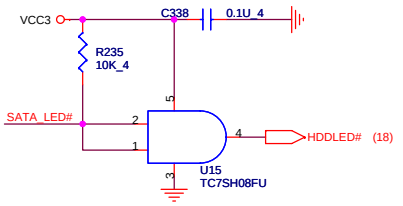
SATA LED



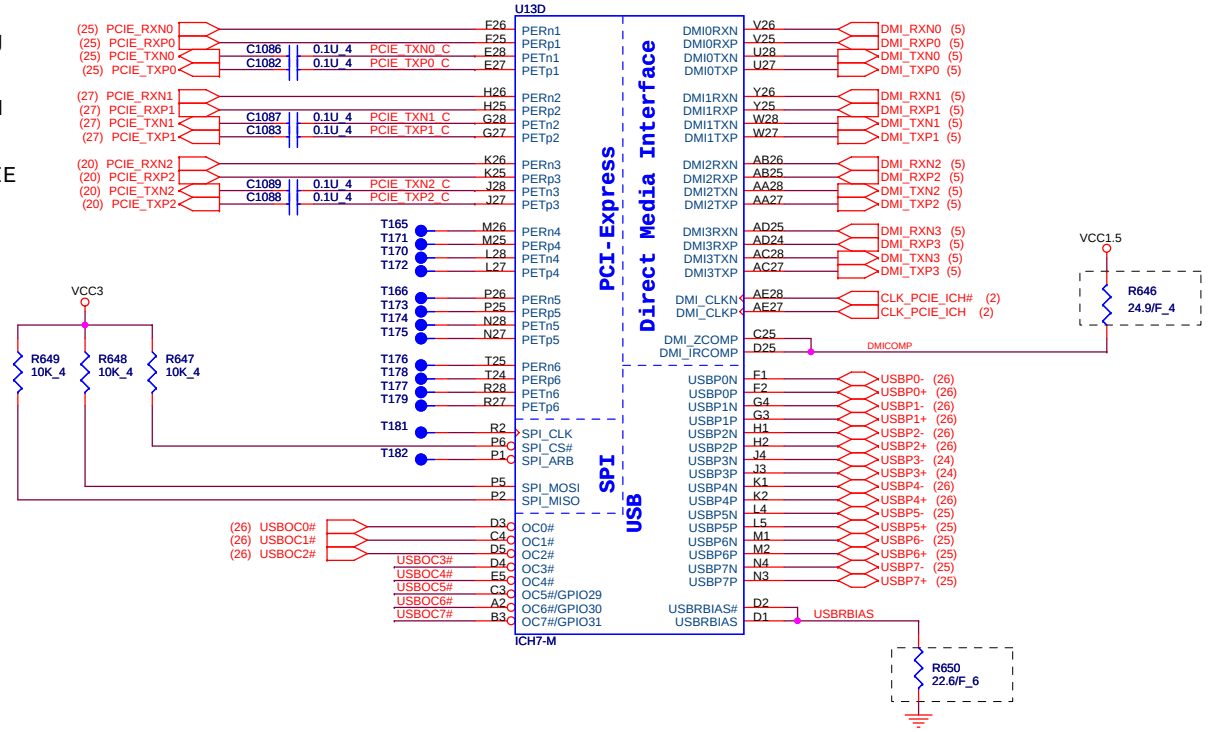
QUANTA COMPUTER

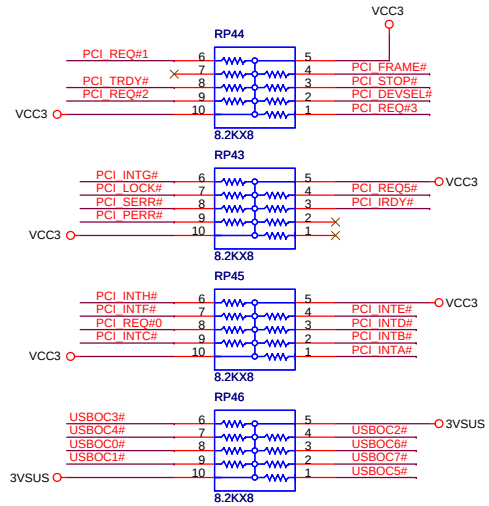
Title	ICH7-M HOST1 of 4	
Size	Document Number: RJ6 Main Board	Rev 2A
Date: Wednesday, May 03, 2006	Sheet 13 of 40	

Docking

Giga LAN

MINI PCIE

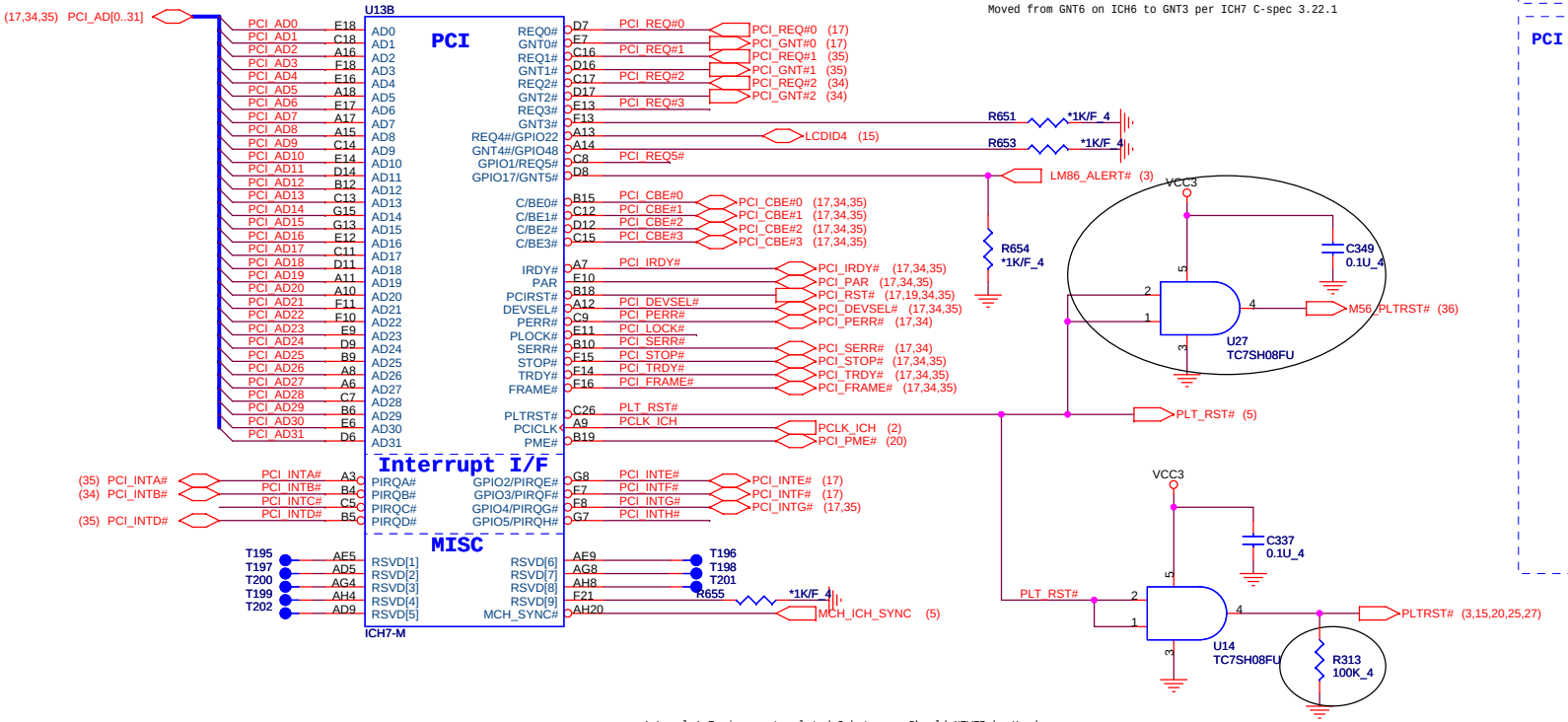




ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

Moved from GNT6 on ICH6 to GNT3 per ICH7 C-spec 3.22.1



PCI bus info.

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ0# / GNT0#	PIRQ E/F/G
Sil3512	AD28	REQ2# / GNT2#	PIRQ B
VT6212	AD27	REQ1# / GNT1#	PIRQ A/D/G

Interrupts	PCI DEVICE		
PIRQA	USB UHCI controller1, 4	VT6212	
PIRQB	Audio and Modem ; option for SMBus	Sil3512	
PIRQC	USB UHCI controller3 ; SATA/IDE Native Mode		
PIRQD	USB UHCI controller2	VT6212	
PIRQE	INT LAN; option for SCI, TCO, HPET#0,1,2	PCI7411	
PIRQF	option for SCI, TCO, HPET#0,1,2	PCI7411	
PIRQG	option for SCI, TCO, HPET#0,1,2	PCI7411	VT6212
PIRQH	USB EHCI controller; option for SCI, TCO, HPET#0,1,2		

1.Level 1 Environment-related Substances Should NEVER be Used.
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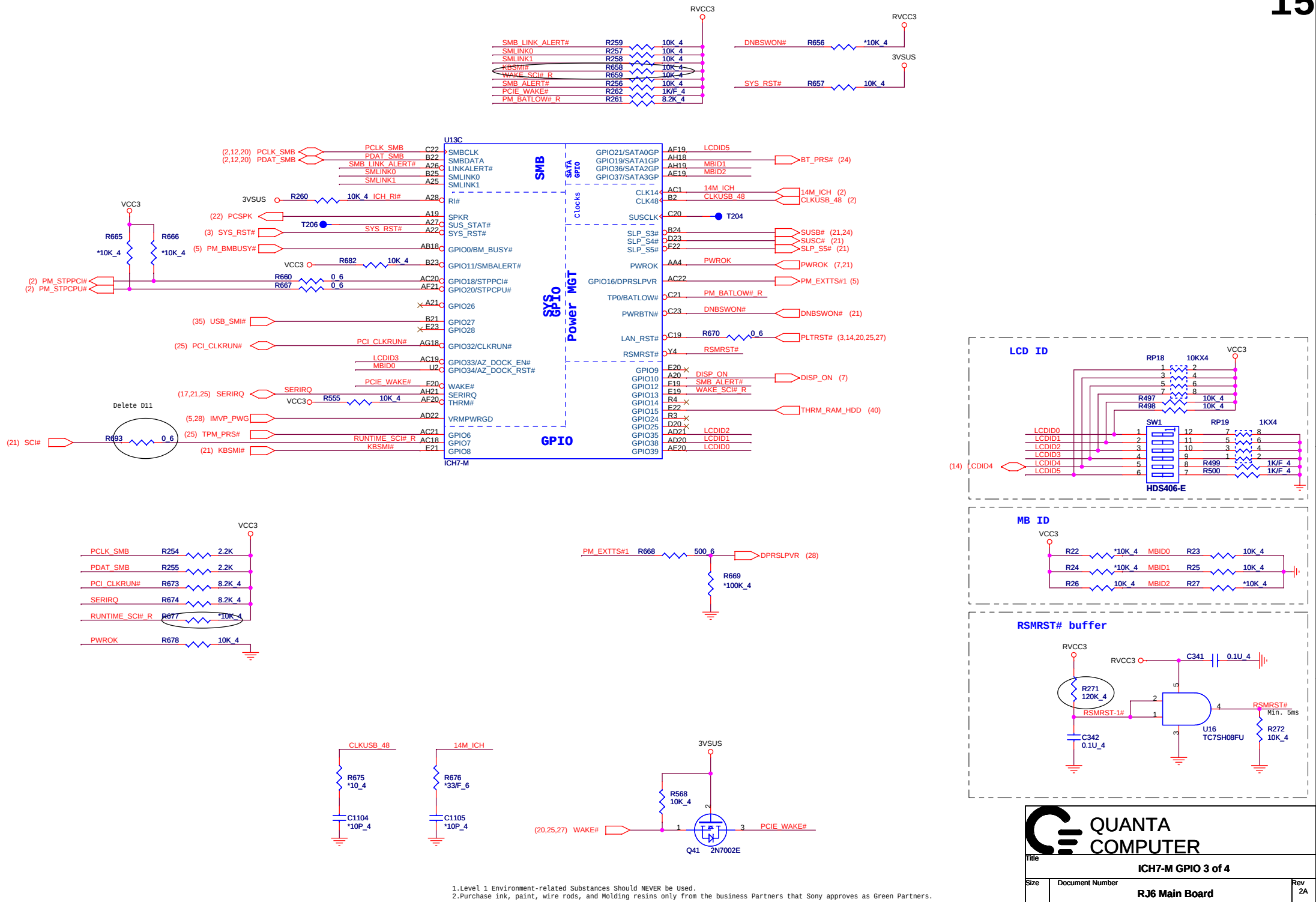
QUANTA COMPUTER

Title	ICH7-M PCIE 2 of 4	
Size	Document Number: RJ6 Main Board	Rev: 1B
Date: Wednesday, May 03, 2006	Sheet 14 of 40	



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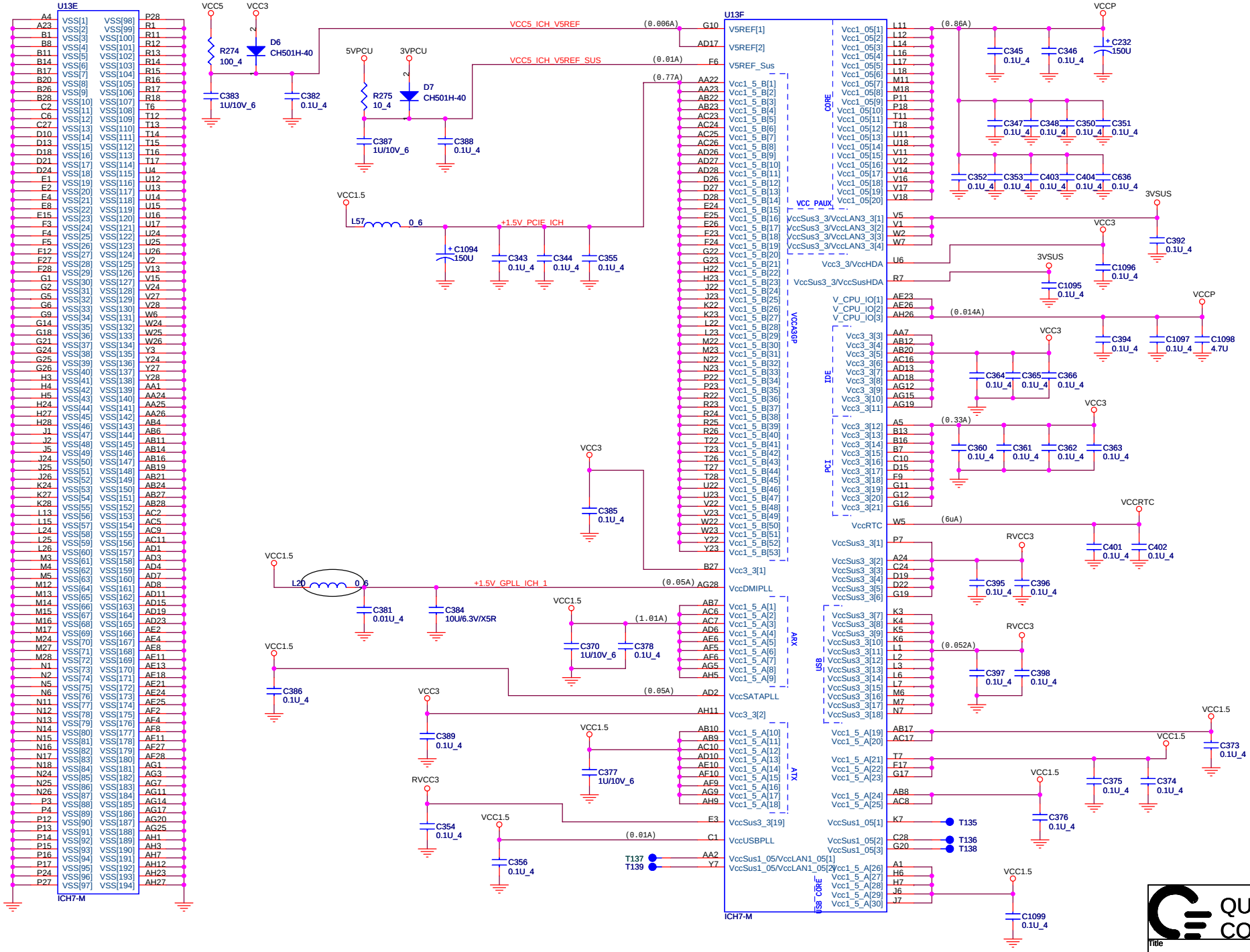
QUANTA COMPUTER

Title	ICH7-M GPIO 3 of 4	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Tuesday, May 09, 2006	Sheet 15 of 40	



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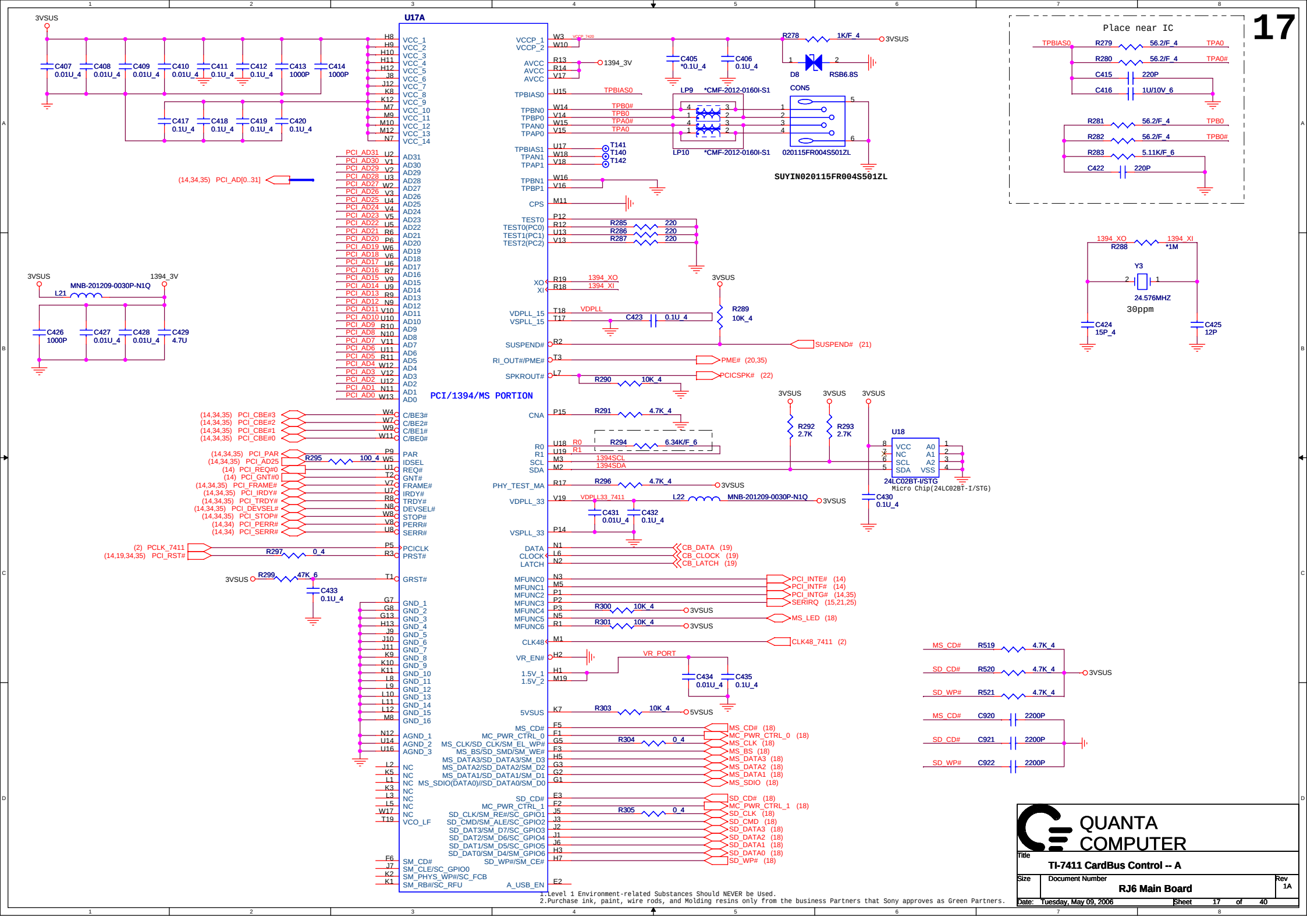
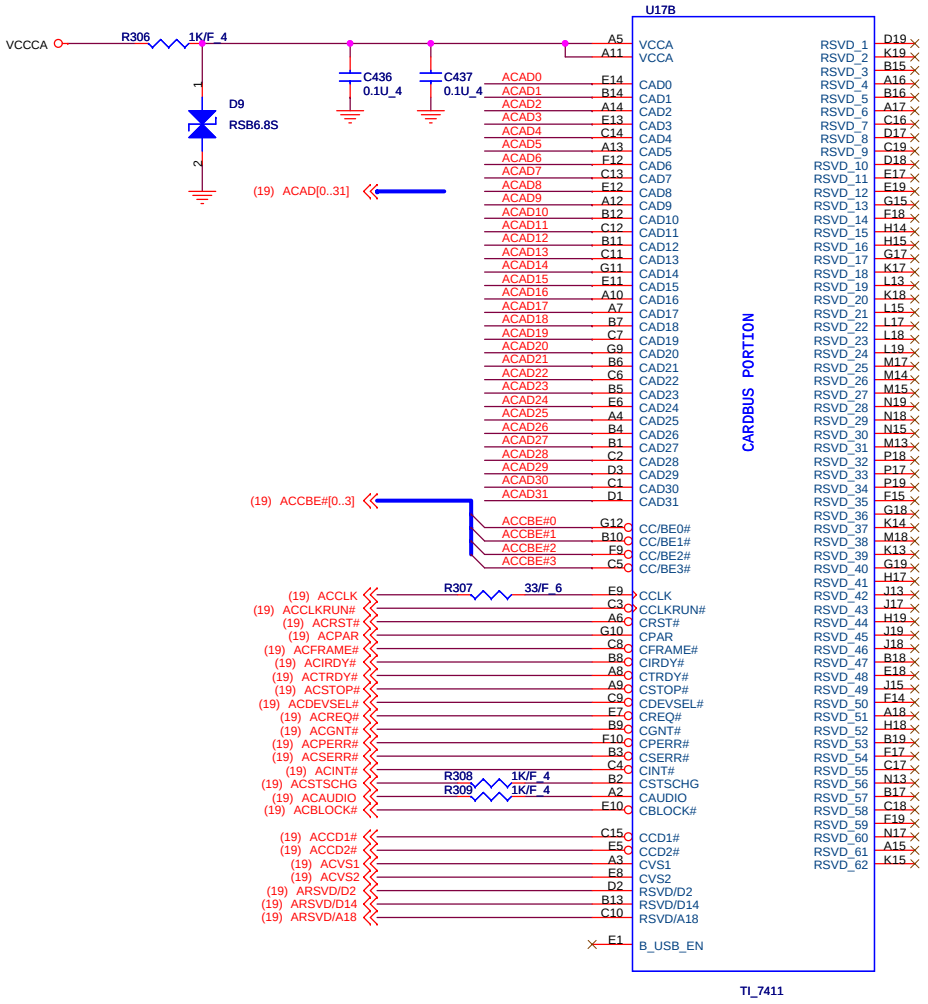
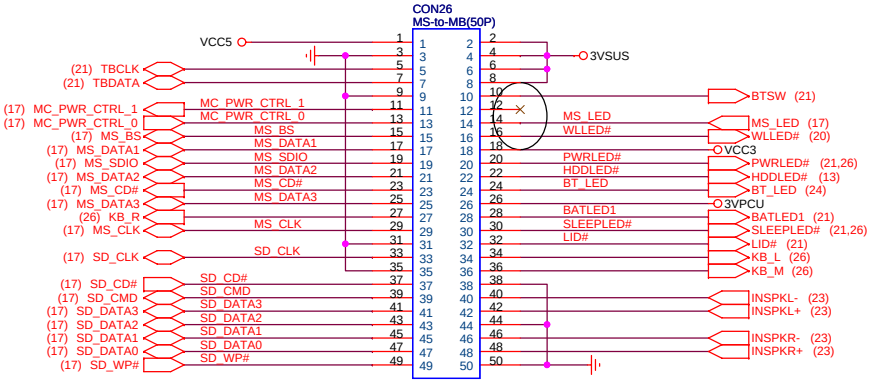
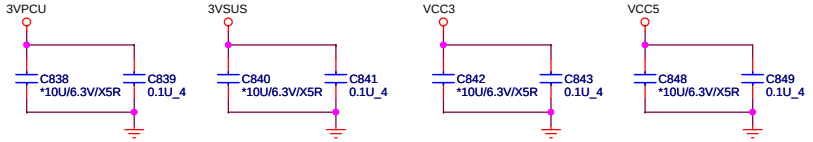
QUANTA COMPUTER

Title	ICH7-M Power 4 o 4	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Wednesday, May 03, 2006	Sheet 16 of 40	


U17A
PCI/1394/MS PORTION
3VSUS
1394_3V
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
C407 0.01U_4
C408 0.01U_4
C409 0.01U_4
C410 0.01U_4
C411 0.1U_4
C412 0.1U_4
C413 1000P
C414 1000P
C417 0.1U_4
C418 0.1U_4
C419 0.1U_4
C420 0.1U_4
(14,34,35) PCI_AD[0..31]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
MNB-201209-0030P-N1Q
L21
C426 1000P
C427 0.01U_4
C428 0.01U_4
C429 4.7U
(14,34,35) PCI_CBE#3
(14,34,35) PCI_CBE#2
(14,34,35) PCI_CBE#1
(14,34,35) PCI_CBE#0
C/BE3# C/BE2# C/BE1# C/BE0#
(14,34,35) PCI_PAR
(14,34,35) PCI_AD25
(14) PCI_REQ#0
(14) PCI_GNT#0
(14,34,35) PCI_FRAME#
(14,34,35) PCI_IRDY#
(14,34,35) PCI_TRDY#
(14,34,35) PCI_DEVSEL#
(14,34,35) PCI_STOP#
(14,34) PCI_PERR#
(14,34) PCI_SERR#
R295 100_4
PAR IDSEL REQ# GNT# FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
(2) PCLK_7411
(14,19,34,35) PCI_RST#
R297 0_4
PCICLK PRST#
3VSUS R299 47K_6 GRST#
C433 0.1U_4
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16
AGND_1 AGND_2 AGND_3
NC NC NC







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QUANTA COMPUTER

Title	TI-7411 CardBus Control -- B	
Size	Document Number: RJ6 Main Board	Rev: 2A
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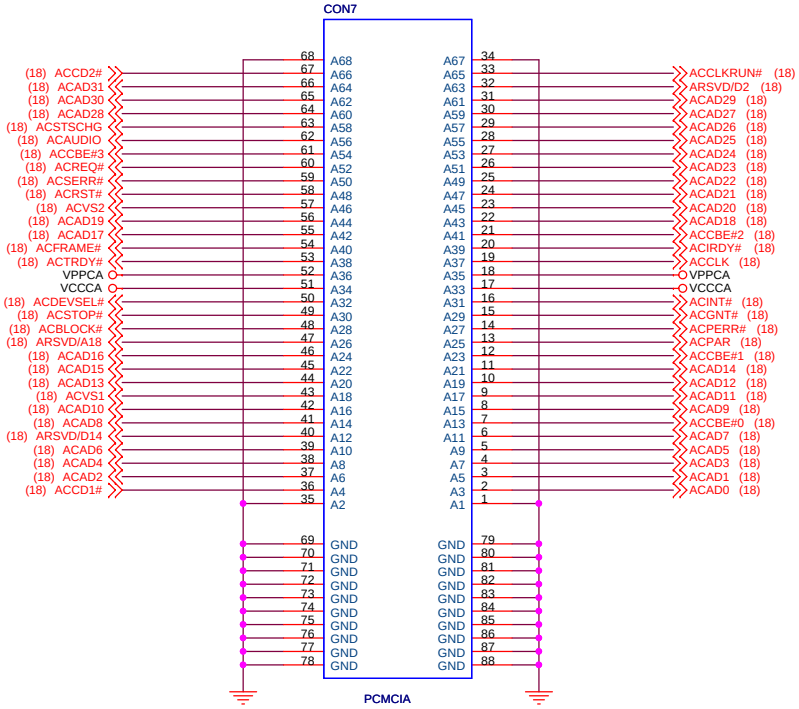
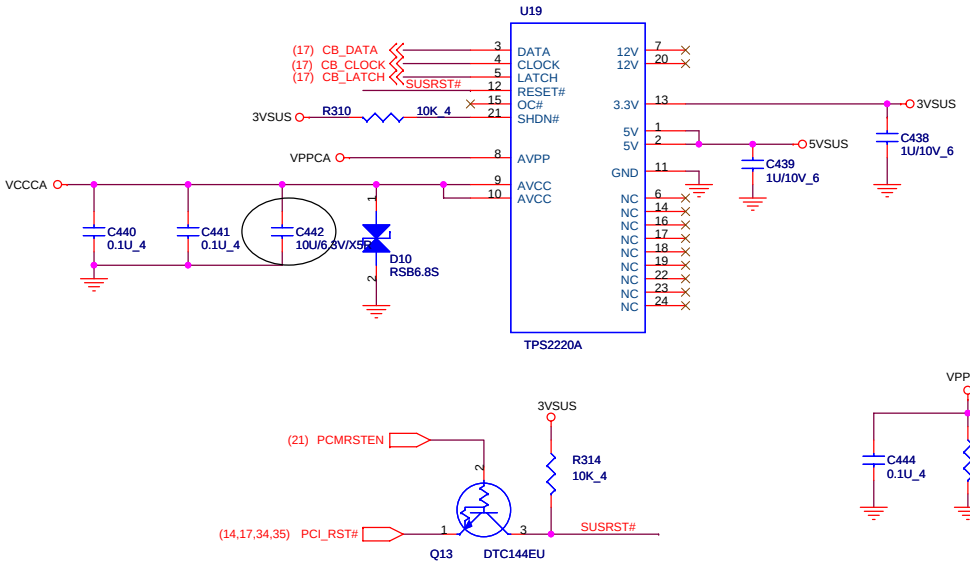
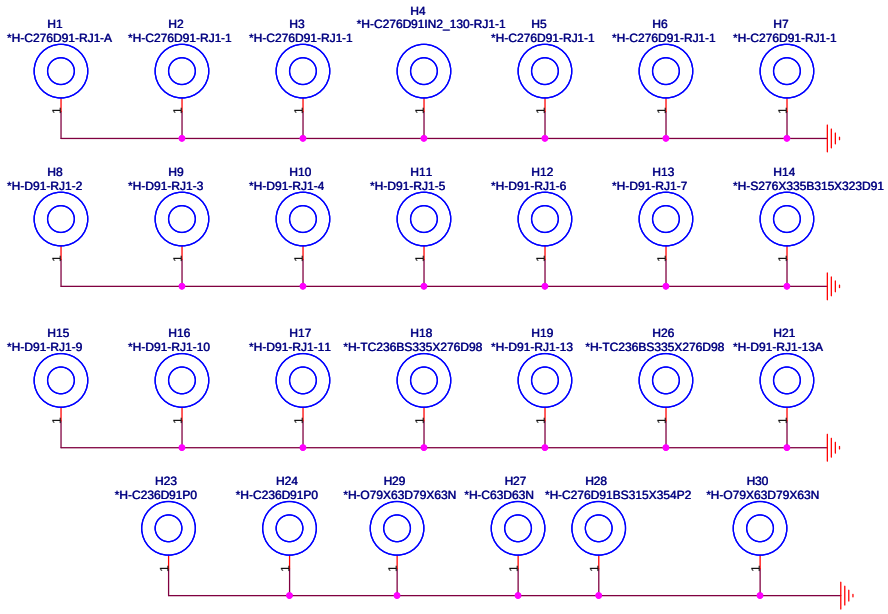
(18) ACAD[0..31]
(18) ACCBE#[0..3]







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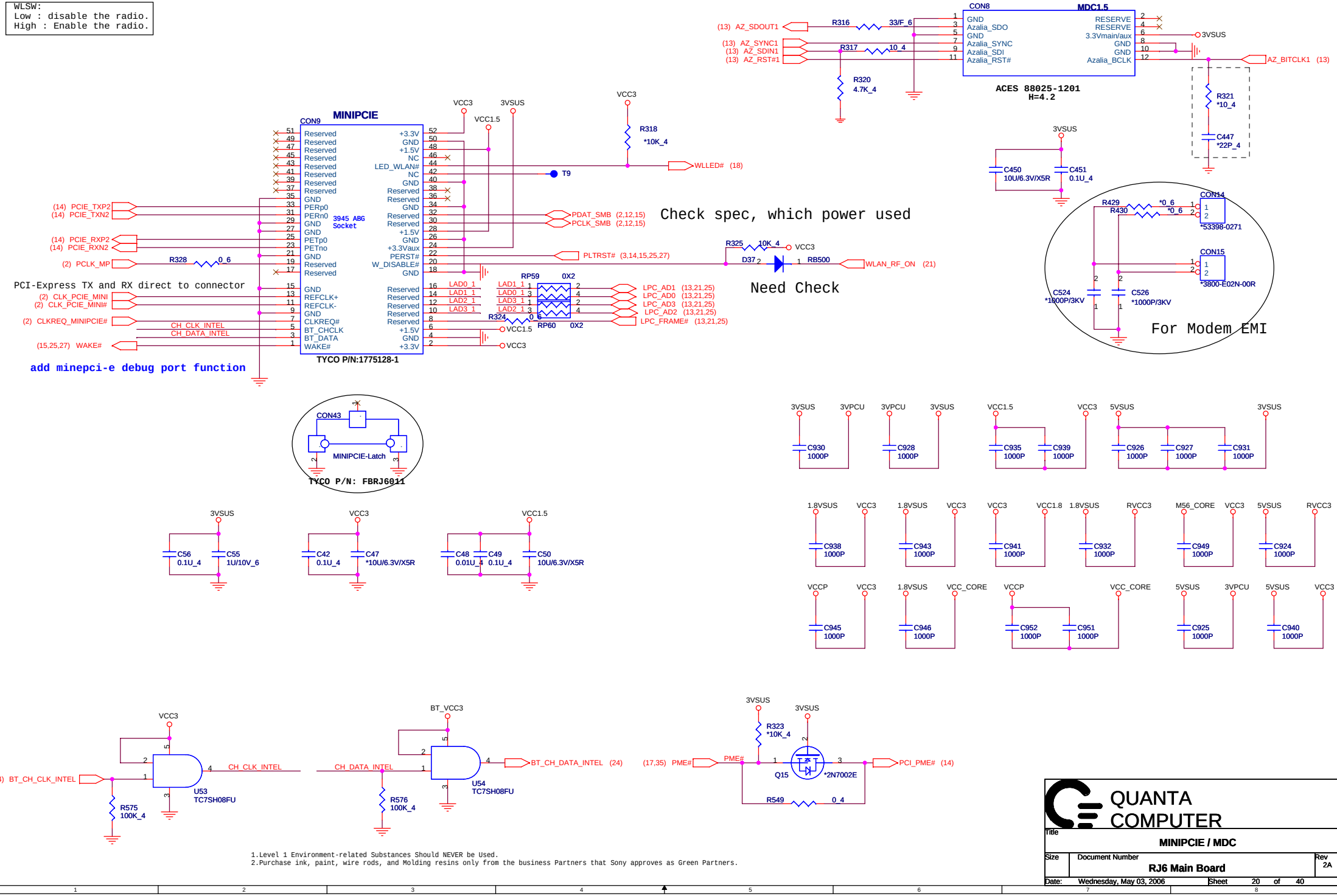
QUANTA COMPUTER

Title	CARDBUS SLOT	
Size	Document Number: RJ6 Main Board	Rev: 1A
Date: Tuesday, May 09, 2006	Sheet 19 of 40	

MDC V1.5

LED_GP :LED WLEN LINK
Output Current : 7mA
Blink rate : 1 flash per every 3 sec.

WLSW:
Low : disable the radio.
High : Enable the radio.



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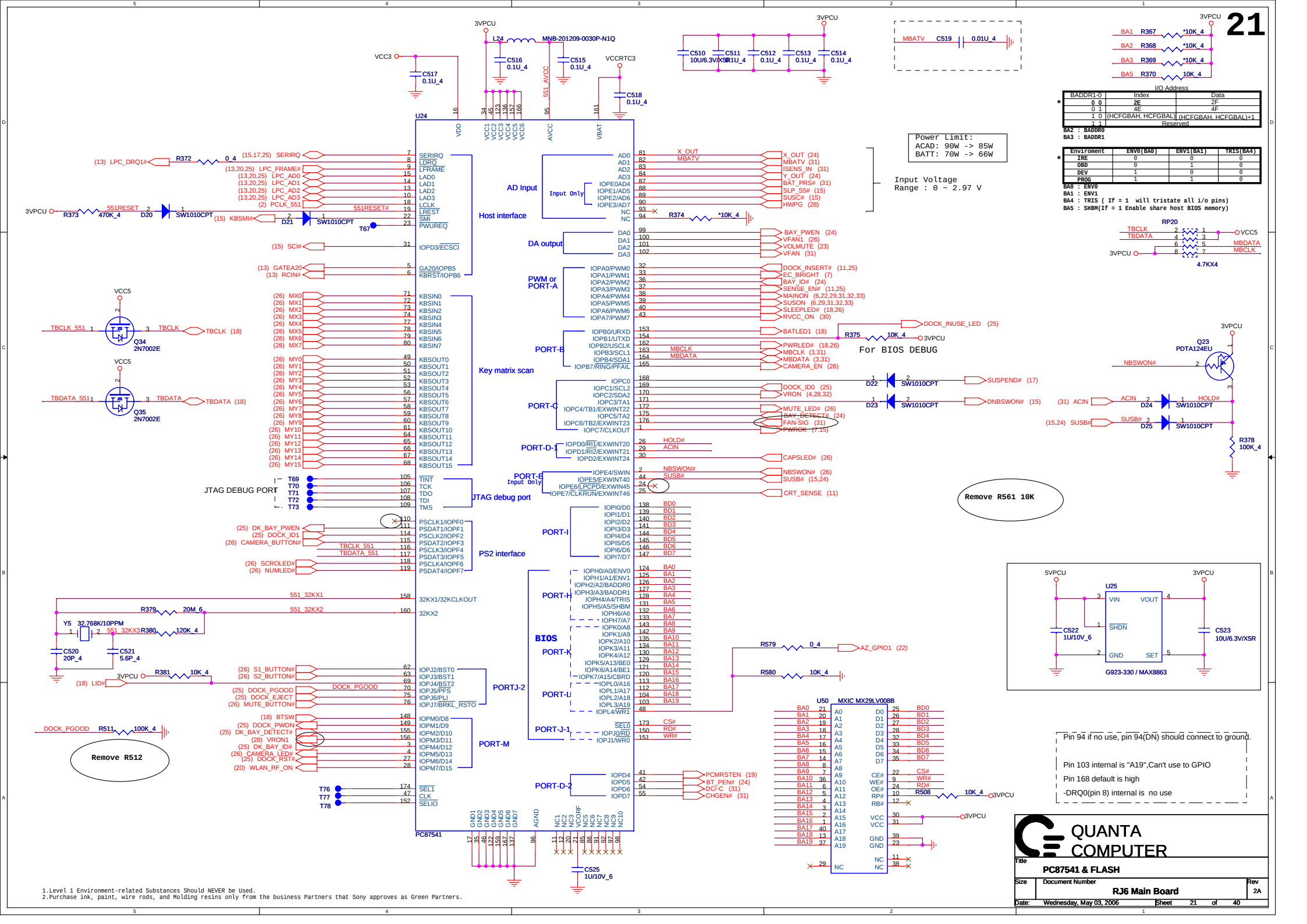
QUANTA COMPUTER

Title	MINIPCIE / MDC	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Wednesday, May 03, 2006	Sheet 20 of 40	


21
U24
PC87541
Power Limit:
ACAD: 90W -> 85W
BATT: 70W -> 66W
Input Voltage
Range : 0 ~ 2.97 V
For BIOS DEBUG
Remove R561 10K
Remove R512
JTAG DEBUG PORT
Host interface
Key matrix scan
PS2 interface
JTAG debug port
BIOS
AD Input
DA output
PWM or PORT-A
PORT-B
PORT-C
PORT-D-1
PORT-E
PORT-I
PORT-H
PORT-K
PORT-L
PORT-J-1
PORT-D-2
PORTJ-2
PORT-M
U50 MXIC MX29LV008B
G923-330 / MAX8863
I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
BA2 : BADDR0
BA3 : BADDR1
Enviroment | ENV0(BA0) | ENV1(BA1) | TRIS(BA4)
IRE | 0 | 0 | 0
OBD | 0 | 1 | 0
DEV | 1 | 0 | 0
PROG | 1 | 1 | 0
BA0 : ENV0
BA1 : ENV1
BA4 : TRIS (If = 1 will tristate all i/o pins)
BA5 : SHBM(If = 1 Enable share host BIOS memory)
Pin 94 if no use, pin 94(DN) should connect to ground.
Pin 103 internal is "A19",Can't use to GPIO
Pin 168 default is high
-DRQ0(pin 8) internal is no use
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.
QUANTA COMPUTER
Title: PC87541 & FLASH
Size: Document Number: RJ6 Main Board
Rev: 2A
Date: Wednesday, May 03, 2006
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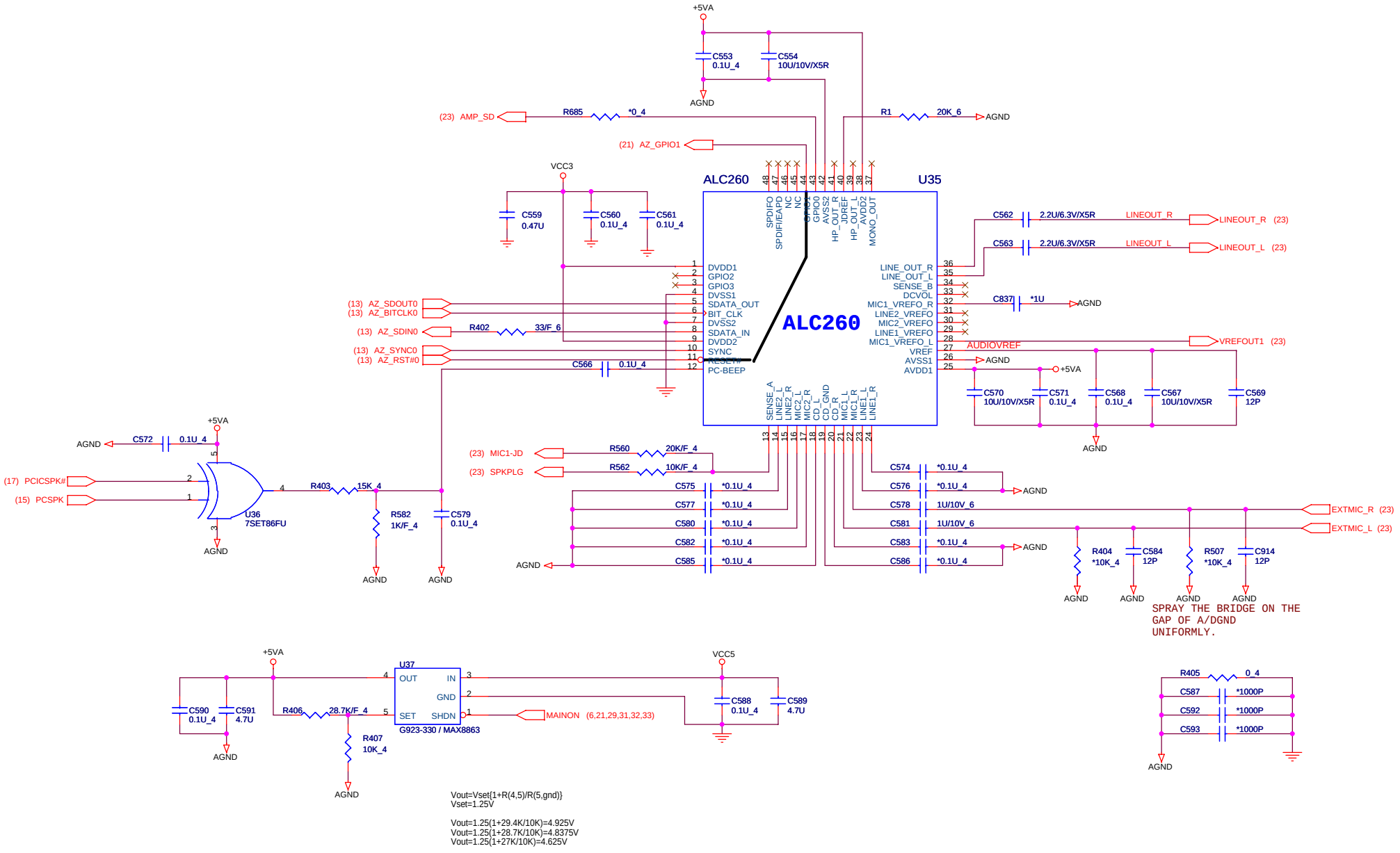

Vout=Vset(1+R(4,5)/R(5,gnd))
Vset=1.25V

Vout=1.25(1+29.4K/10K)=4.925V
Vout=1.25(1+28.7K/10K)=4.8375V
Vout=1.25(1+27K/10K)=4.625V

1.Level 1 Environment-related Substances Should NEVER be Used.
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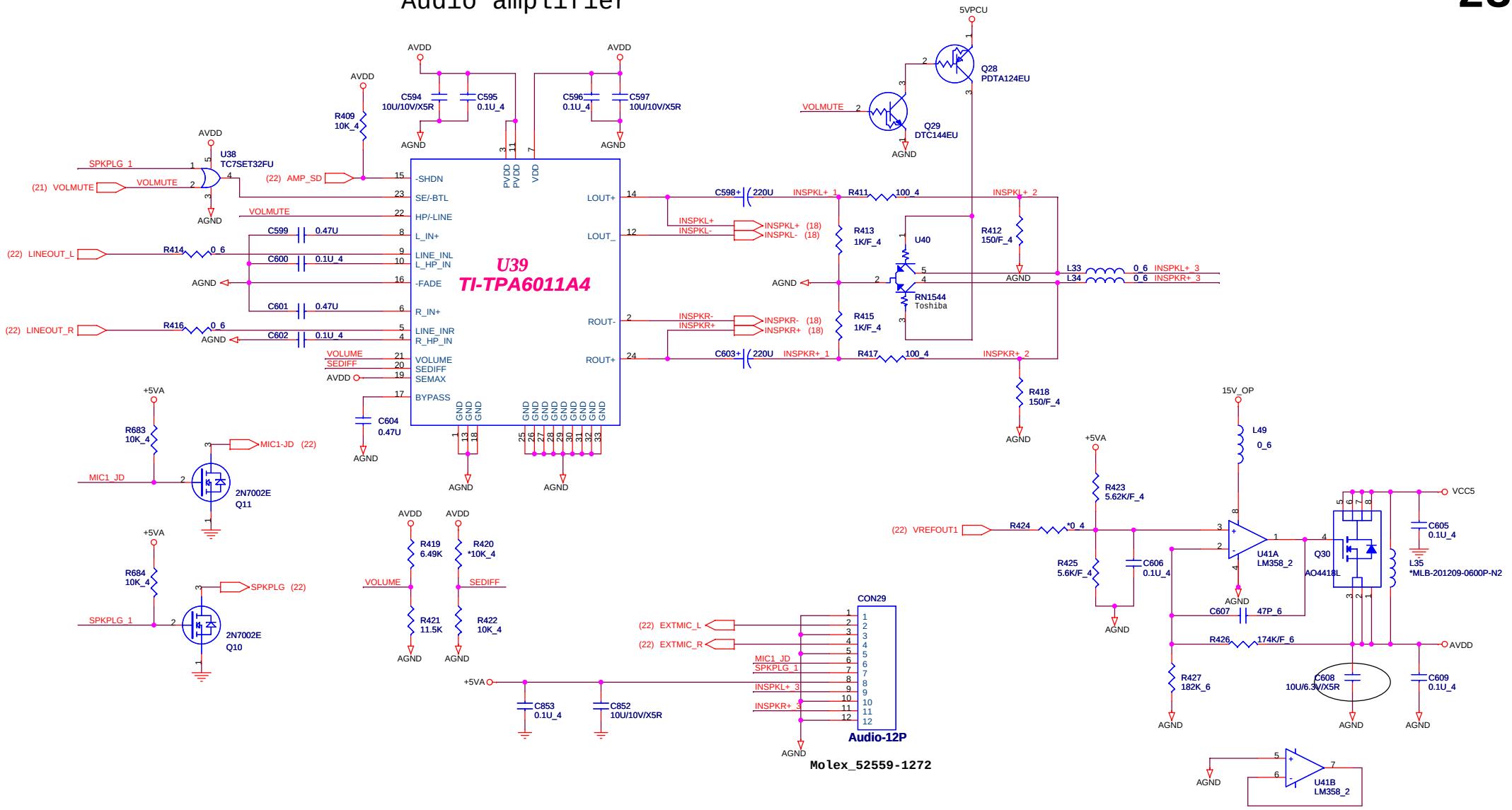
QUANTA COMPUTER

Title	Audio ALC260	
Size	Document Number: RJ6 Audio Board	Rev 1B
Date: Tuesday, May 09, 2006	Sheet 22 of 40	

Audio amplifier



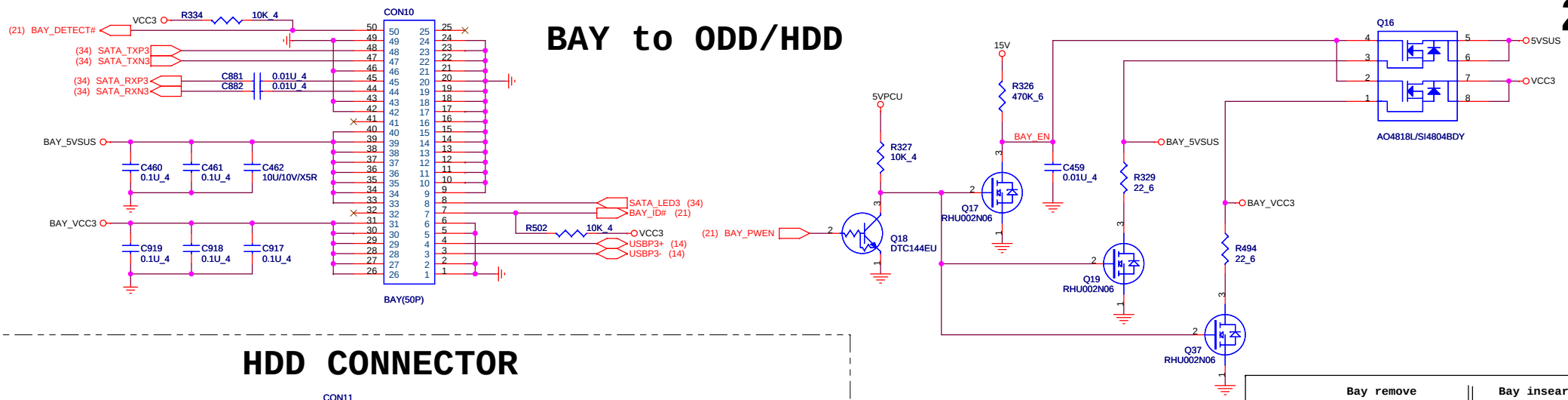
R419	FROM	TO	GAIN
7.5K	2.85	2.89	8 dB
* 6.49K	2.96	3.0	10 dB

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

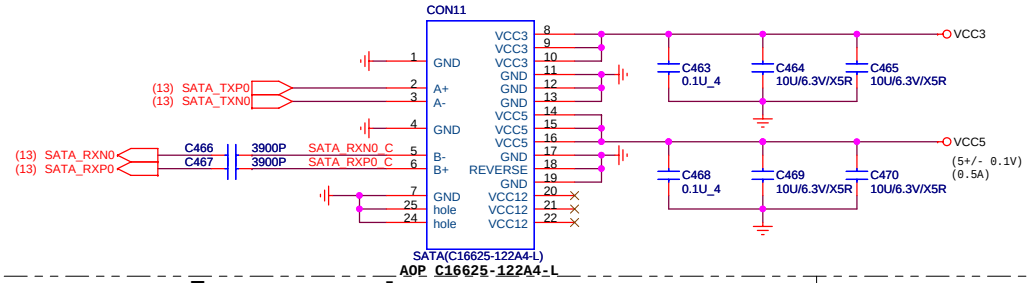
QUANTA COMPUTER

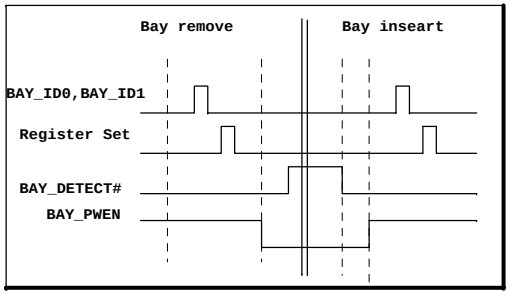
Title: AUDIO AMP		
Size	Document Number: RJ6 Audio Board	Rev: 1B
Date: Tuesday, May 09, 2006	Sheet 23 of 40	

BAY to ODD/HDD



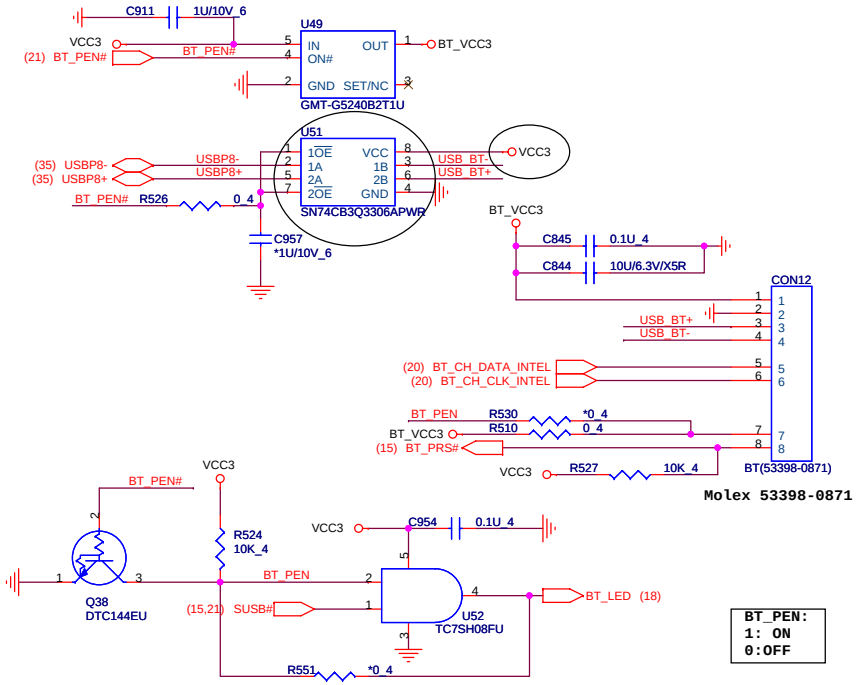
HDD CONNECTOR





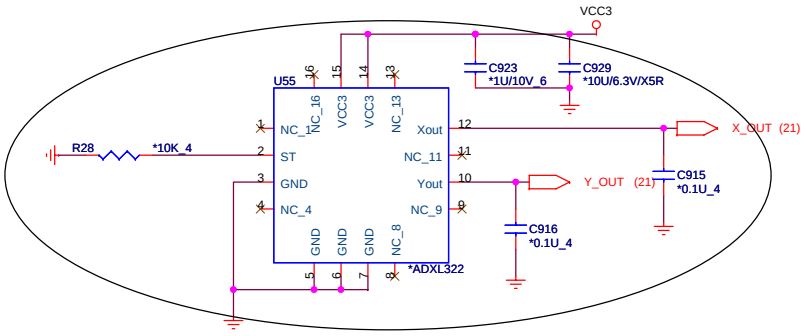
BAY_ID#	
0	SATA Device
1	USB Device

Bluetooth



BT_PEN:
1: ON
0:OFF

Remove WWAN circuit (con36,R506,D28,D27,C912,C910,C913)(P24)



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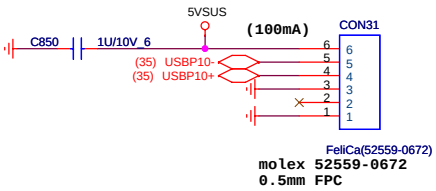
FeliCa

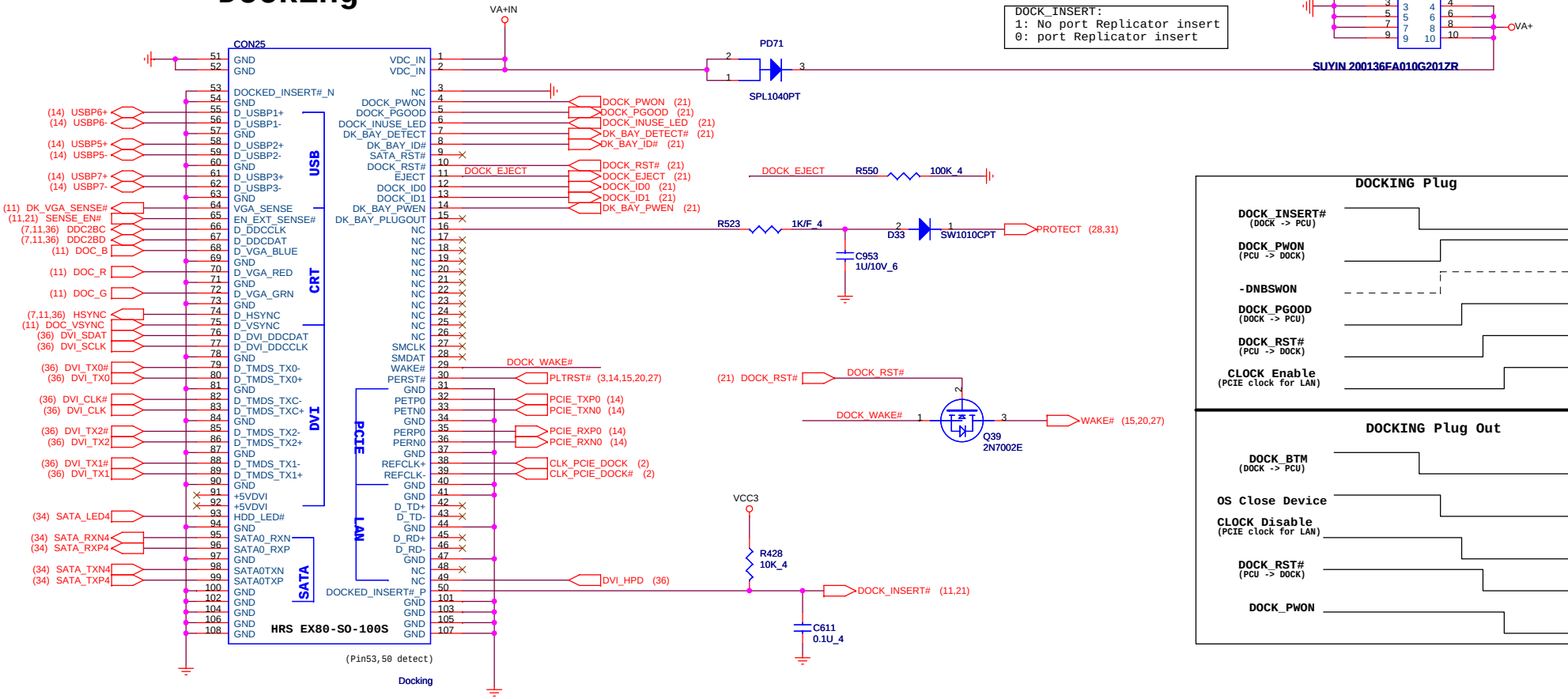


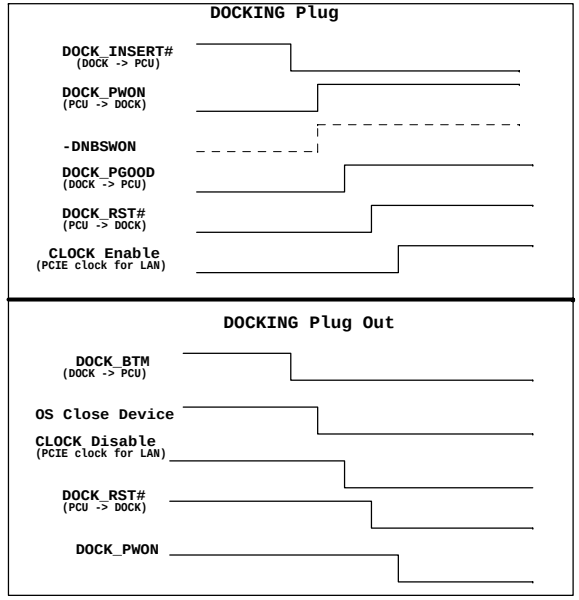
Felica: Molex 52689-0693

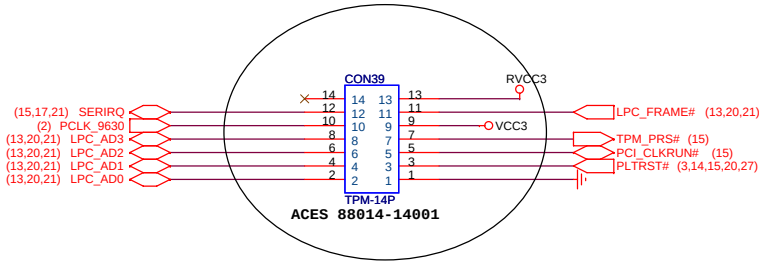
QUANTA COMPUTER

Title	HDD/BAY/BT	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Tuesday, May 09, 2006	Sheet 24 of 40	

Docking





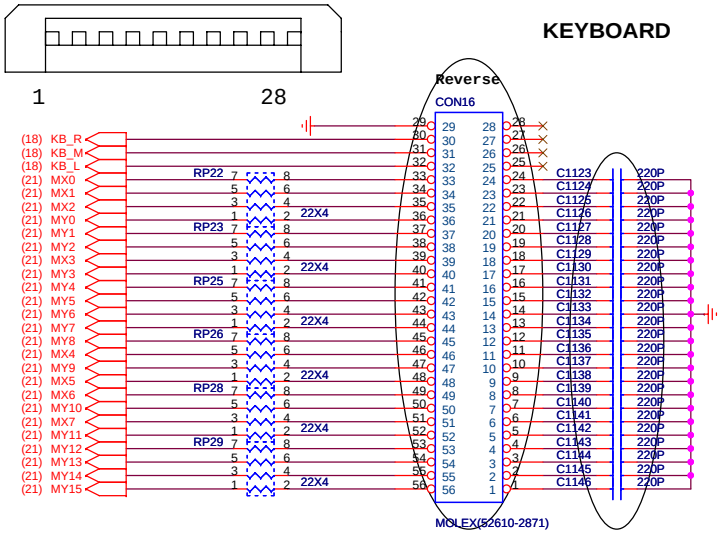


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

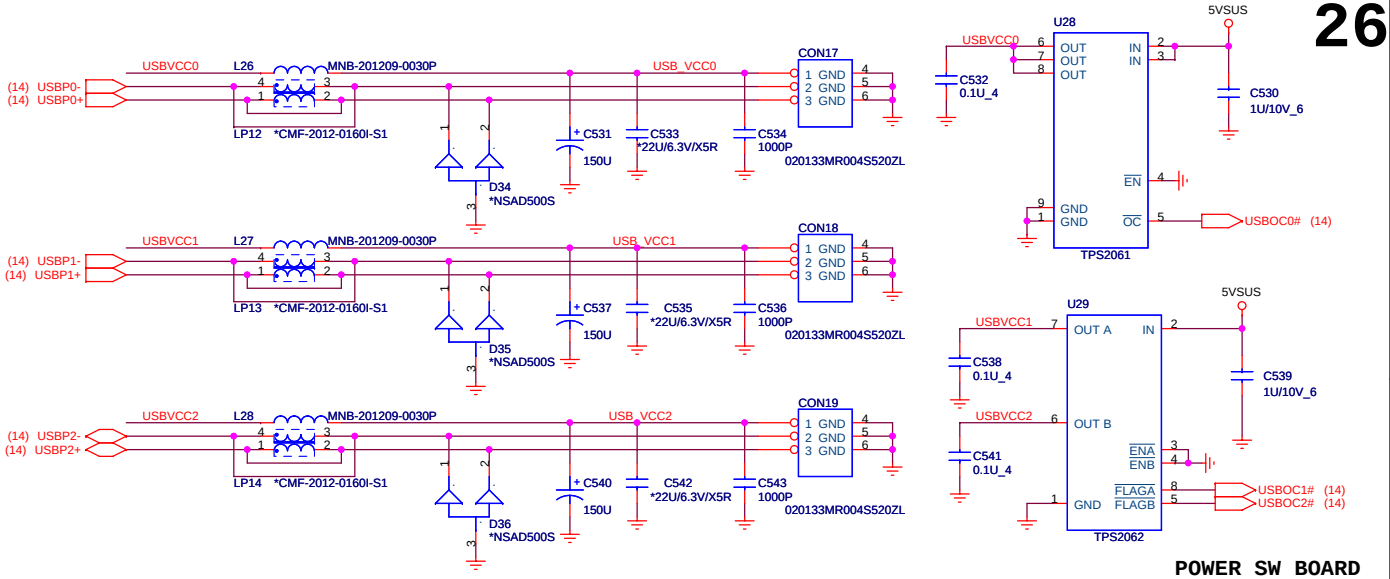
Title	Docking/TPM	
Size	Document Number: RJ6 Main Board	Rev: 1A
Date: Wednesday, May 03, 2006	Sheet 25 of 40	

KEYBOARD

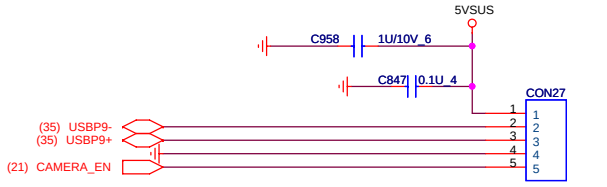


Molex 52610-2871

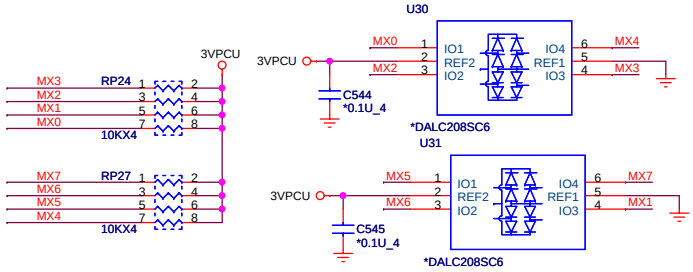
POWER SW BOARD

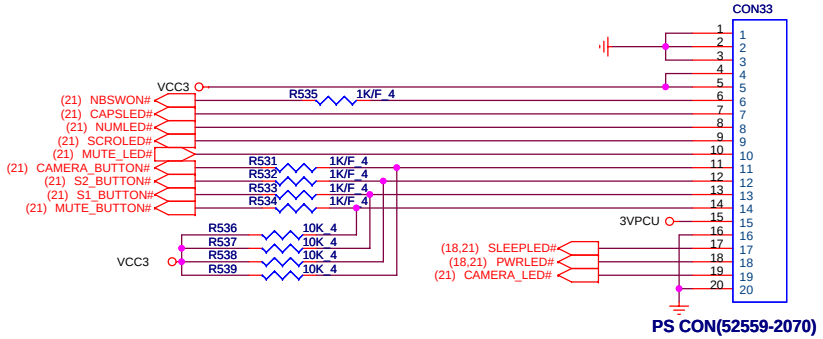


USB Camera

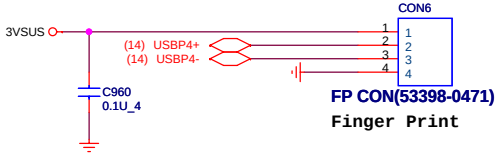


Camera(53398-0571)
Molex 53398-0571



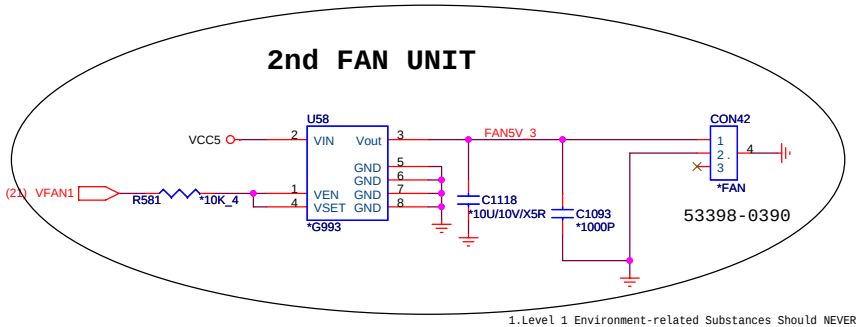


PS CON(52559-2070)
Molex_52559-2070



FP CON(53398-0471)
Finger Print

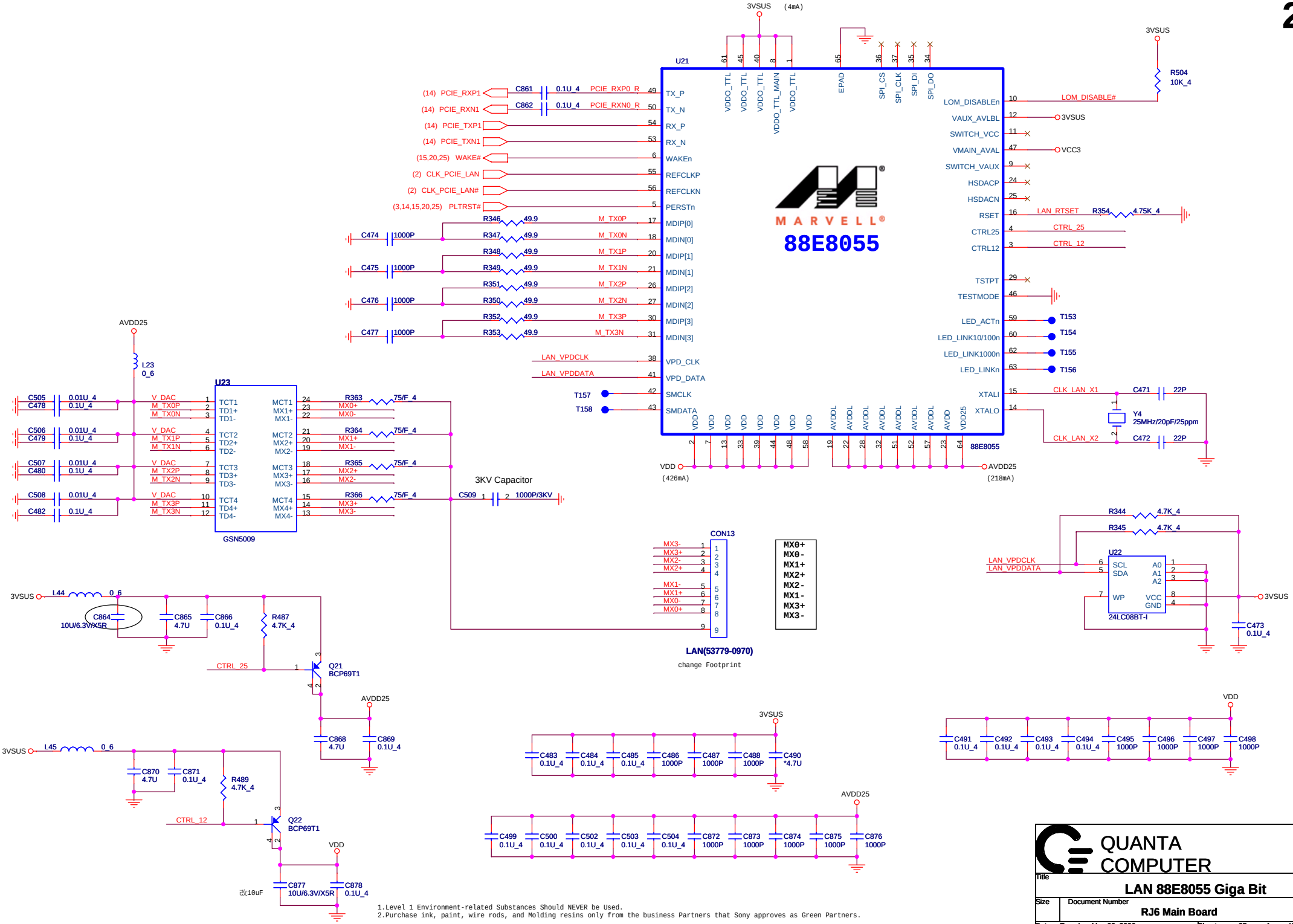
2nd FAN UNIT



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	K/B ,USB	
Size	Document Number: RJ6 Main Board	Rev: 2A
Date: Wednesday, May 03, 2006	Sheet 26 of 40	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	LAN 88E8055 Giga Bit	
Size	Document Number: RJ6 Main Board	Rev: 1B
Date: Tuesday, May 09, 2006	Sheet 27 of 40	

For MAX8770 pass 2: mount PR64, PQ59, PC79
For MAX8770 pass 3: only mount PR65

fsw: 297.8kHz

load line slope: -2.1mV/A

slewrate 12.5mV/us

I_limit = 19.5A

max. 36A

Height should be less than 2.5mm

Near IC

I_limit = 19.5A

Height should be less than 2.5mm

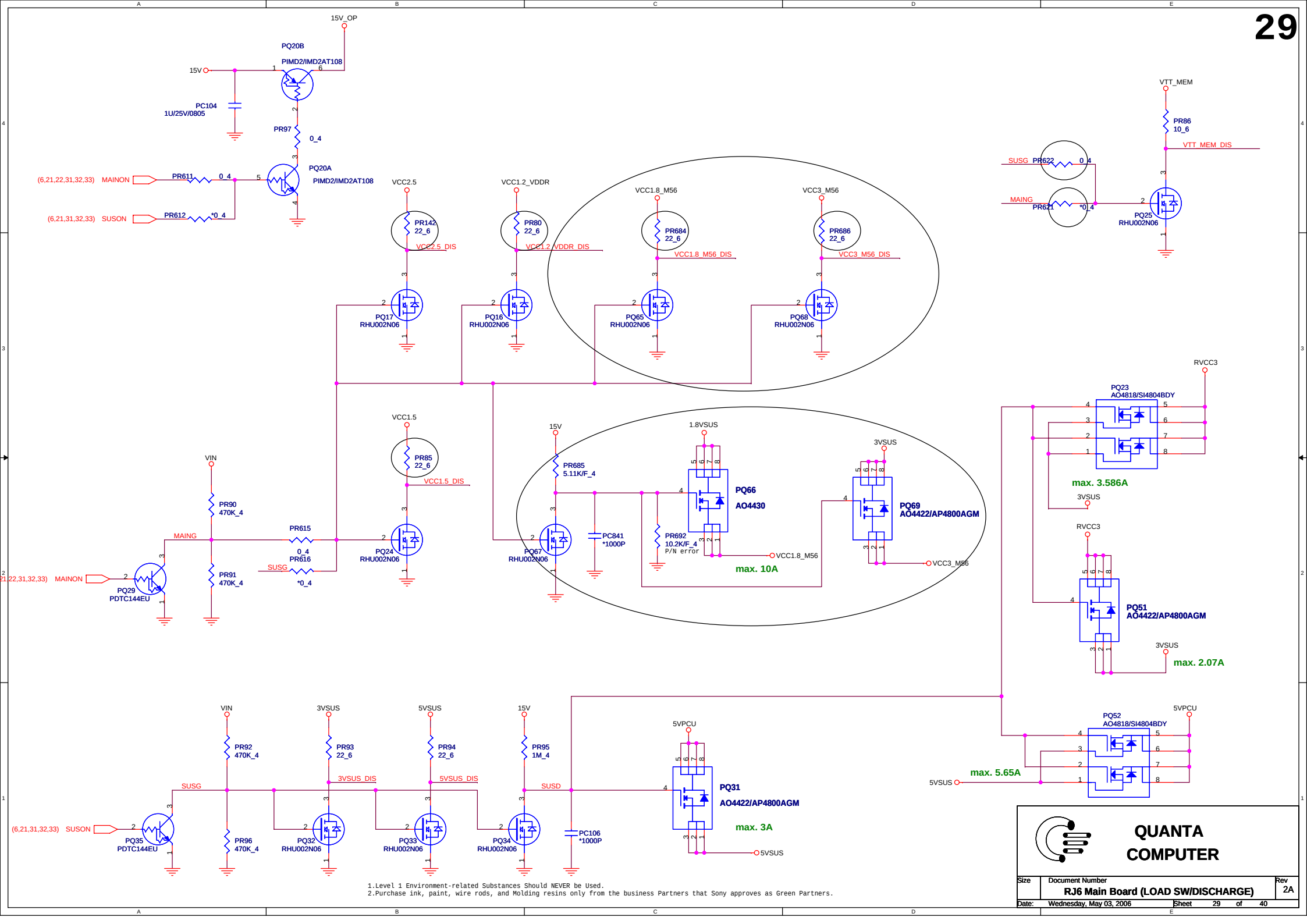
Near IC

M56_D3_HOT_NEED_MOUNT,D3_COLD_NEED_REMOVE

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

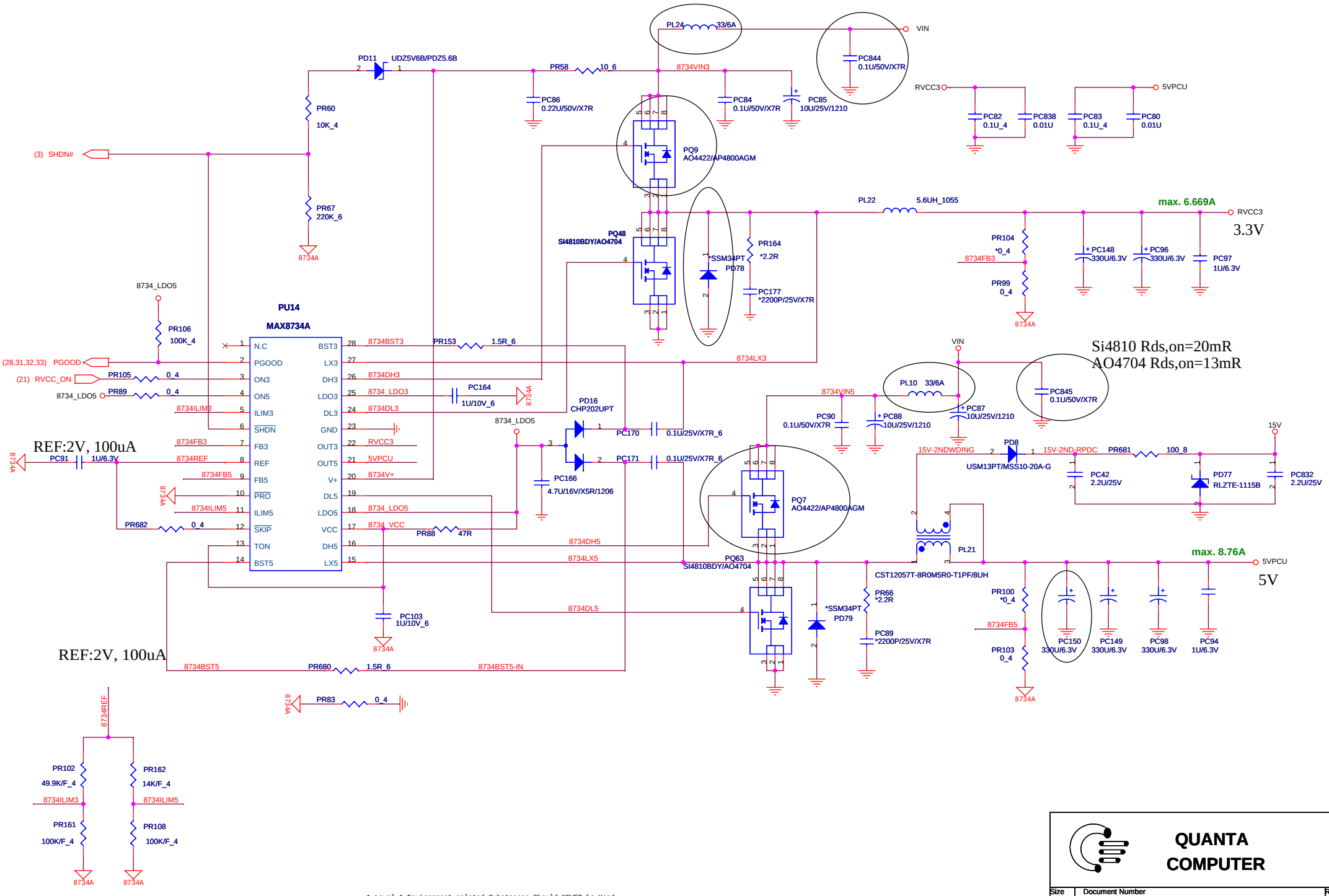
Size	Document Number	Rev
	RJ6 Main Board (VCC_CORE)	2A
Date: Friday, May 05, 2006	Sheet 28 of 40	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

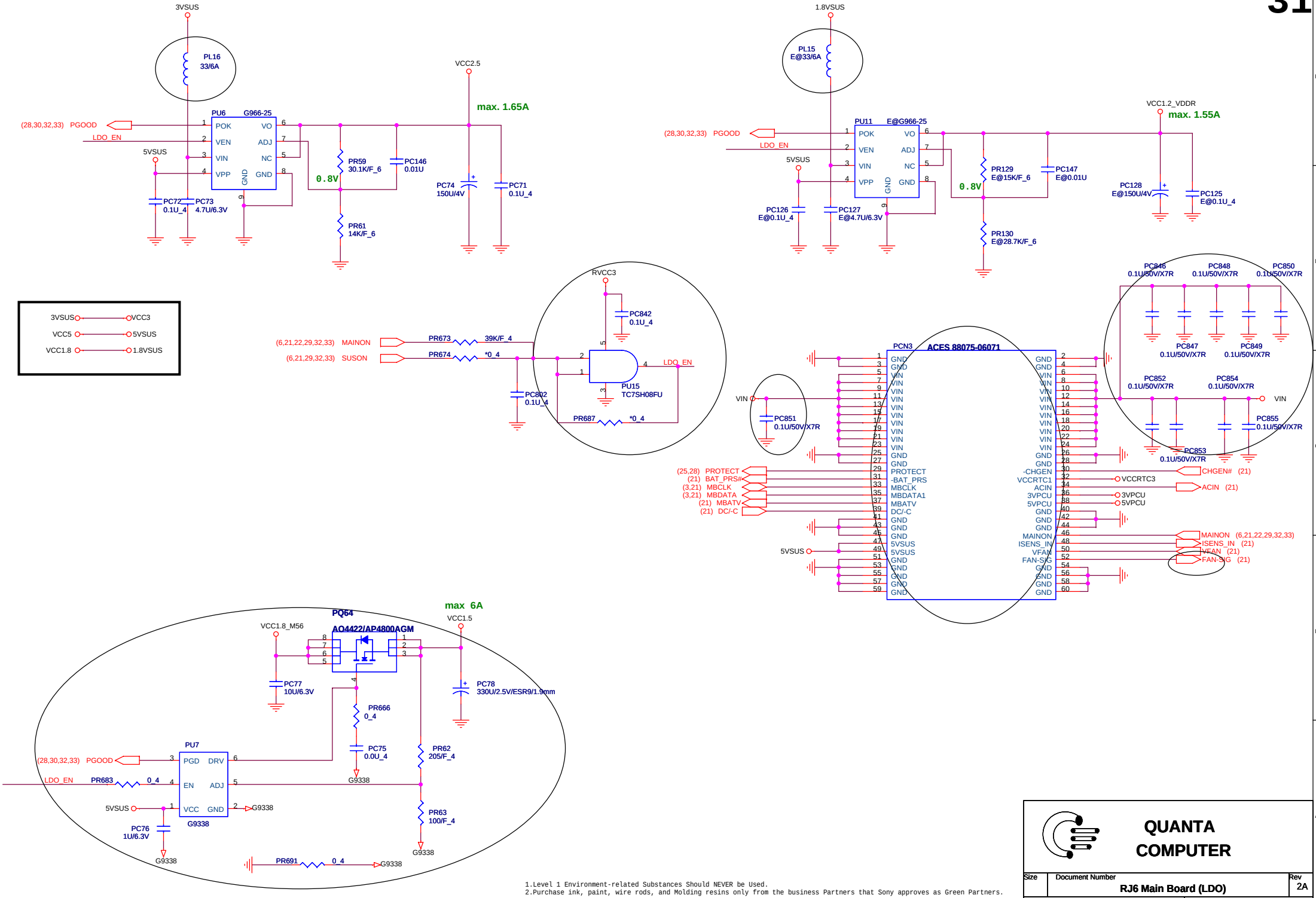
Size	Document Number	Rev
	RJ6 Main Board (LOAD SW/DISCHARGE)	2A
Date: Wednesday, May 03, 2006	Sheet 29 of 40	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

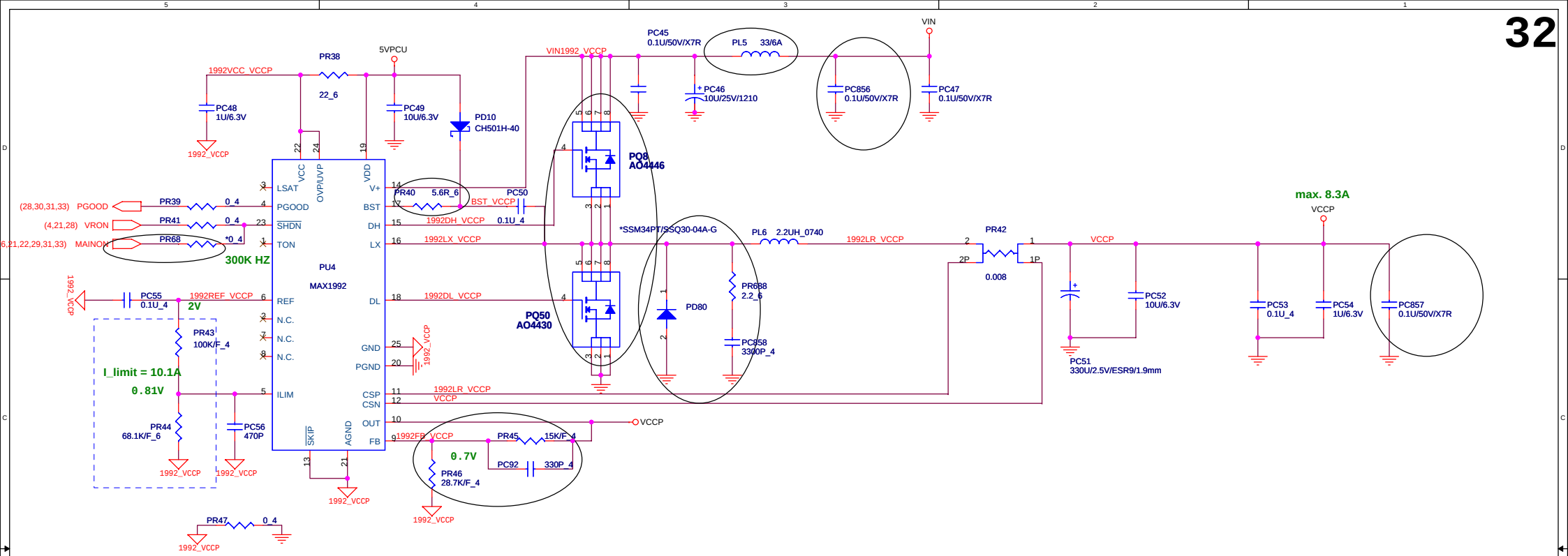
Size	Document Number	Rev
	RJ6 Main Board (5V/3V/12V)	1B
Date: Friday, May 05, 2006	Sheet 30 of 40	

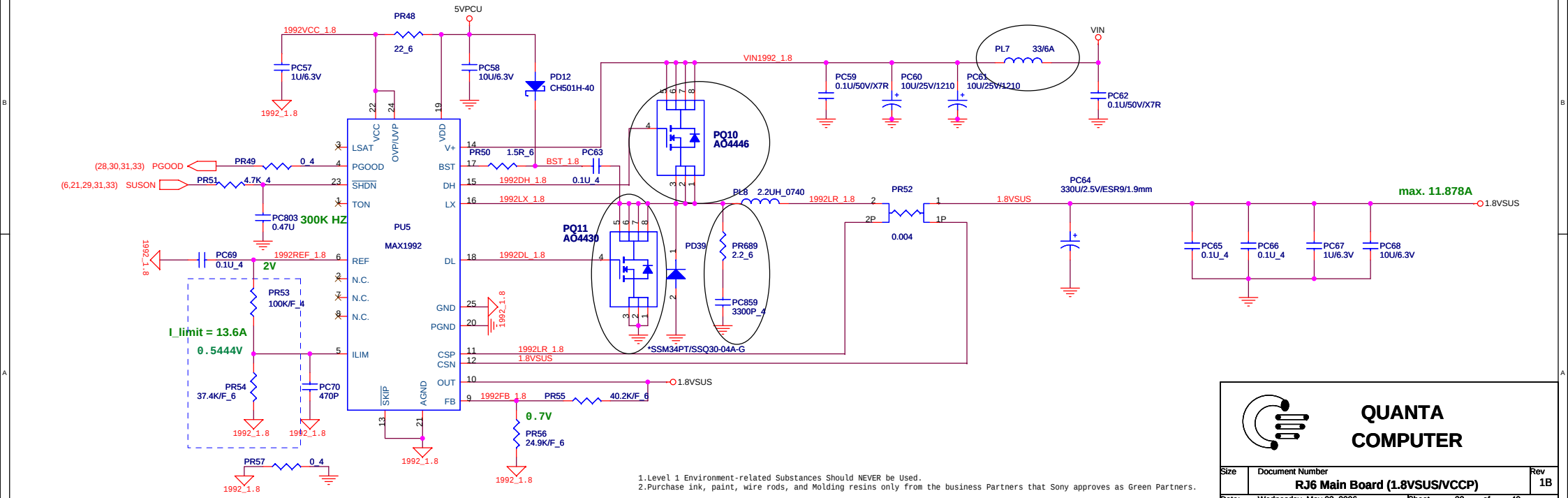


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Size	Document Number	Rev
	RJ6 Main Board (LDO)	2A
Date: Monday, May 08, 2006	Sheet 31 of 40	

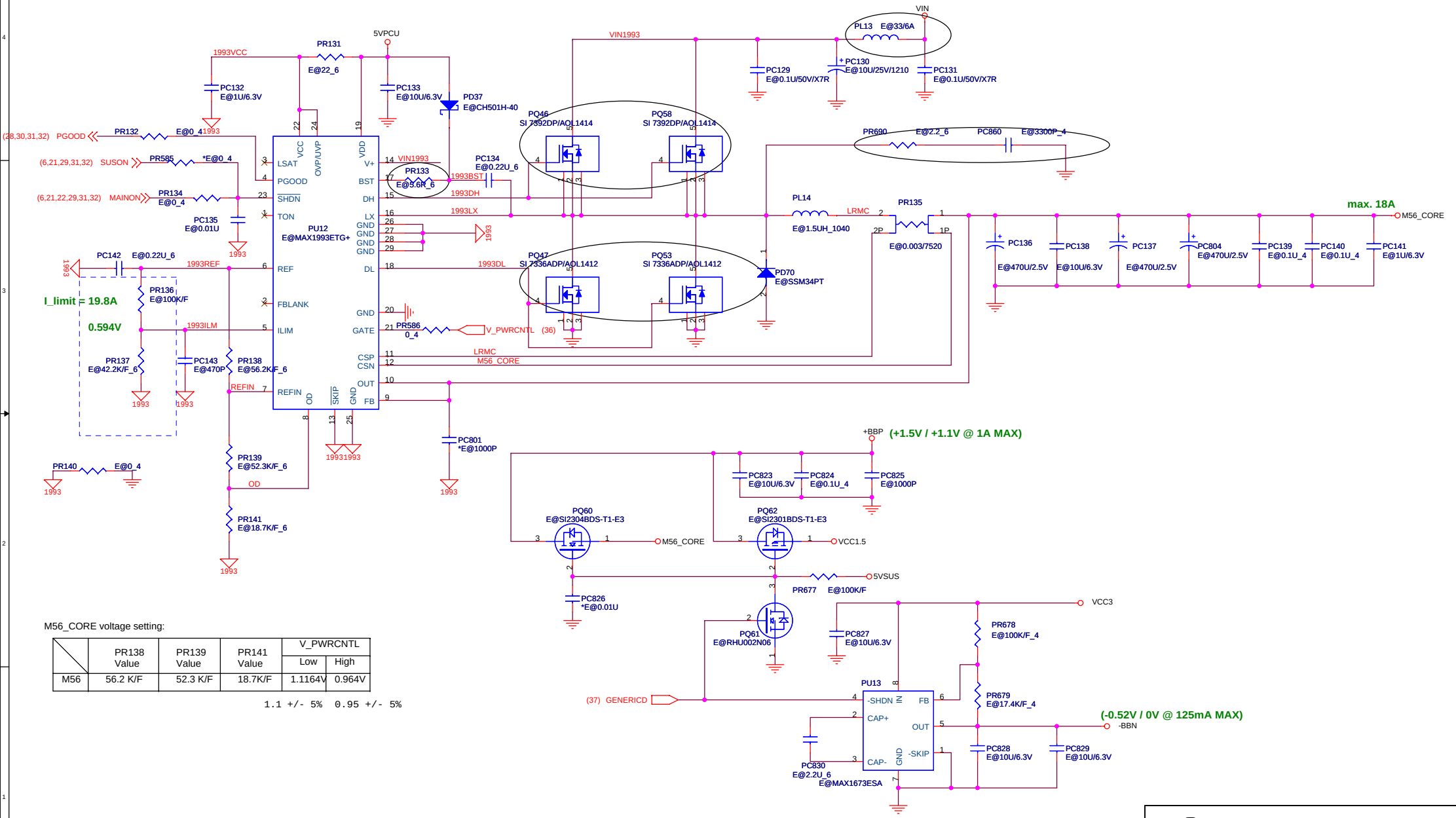




1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Size	Document Number	Rev
	RJ6 Main Board (1.8VSUS/VCCP)	1B
Date: Wednesday, May 03, 2006	Sheet 32 of 40	



M56_CORE voltage setting:

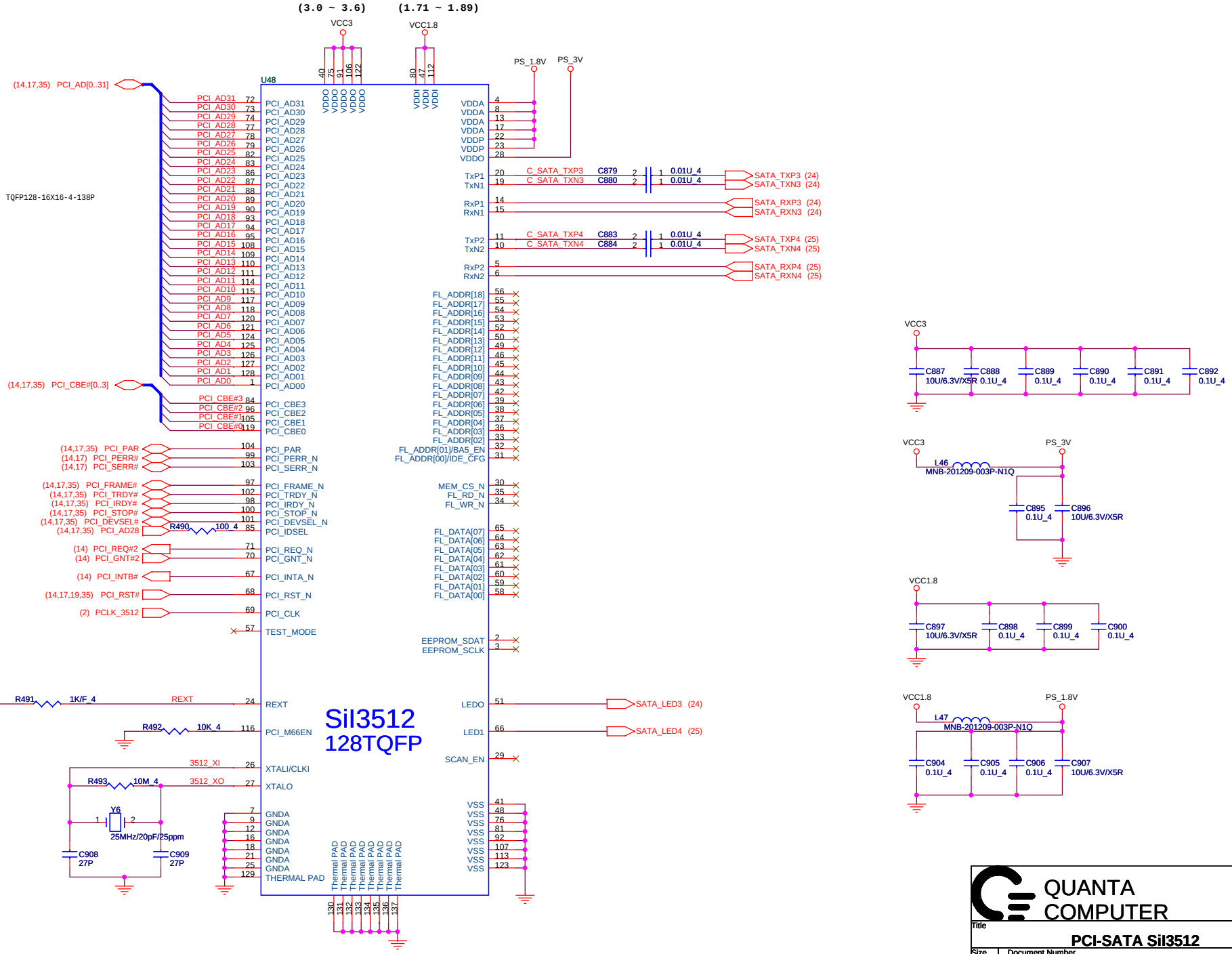
	PR138 Value	PR139 Value	PR141 Value	V_PWRCNTL	
				Low	High
M56	56.2 K/F	52.3 K/F	18.7K/F	1.1164V	0.964V

1.1 +/- 5% 0.95 +/- 5%

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

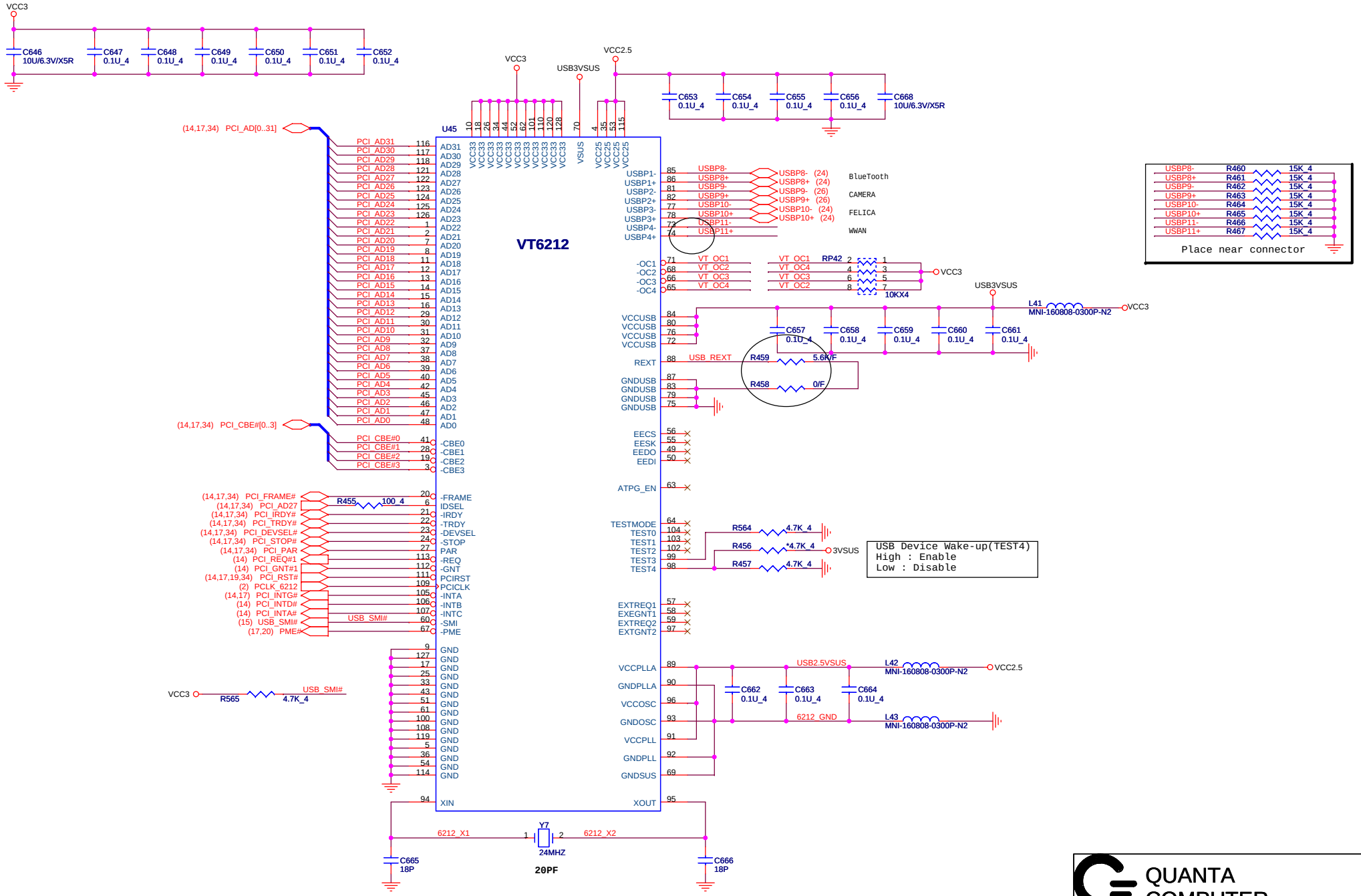
Size	Document Number	Rev
	RJ6 Main Board (M56_CORE)	2A
Date: Wednesday, May 03, 2006	Sheet 33 of 40	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	PCI-SATA Sil3512	
Size: Custom	Document Number: RJ6 Main Board	Rev: 1B
Date: Tuesday, May 09, 2006	Sheet 34 of 40	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	USB Controller VT6212	
Size: Custom	Document Number: RJ6 Main Board	Rev: 2A
Date: Tuesday, May 09, 2006	Sheet 35 of 40	

U3001A

PART 1 OF 7

PCI-EXPRESS INTERFACE

PCIE_RX0P AJ31 / PCIE_RX0N AH31 ← GFX_TXP0 / GFX_TXN0
PCIE_RX1P AH30 / PCIE_RX1N AG30 ← GFX_TXP1 / GFX_TXN1
PCIE_RX2P AG32 / PCIE_RX2N AF32 ← GFX_TXP2 / GFX_TXN2
PCIE_RX3P AF31 / PCIE_RX3N AE31 ← GFX_TXP3 / GFX_TXN3
PCIE_RX4P AE30 / PCIE_RX4N AD30 ← GFX_TXP4 / GFX_TXN4
PCIE_RX5P AD32 / PCIE_RX5N AC32 ← GFX_TXP5 / GFX_TXN5
PCIE_RX6P AC31 / PCIE_RX6N AB31 ← GFX_TXP6 / GFX_TXN6
PCIE_RX7P AB30 / PCIE_RX7N AA30 ← GFX_TXP7 / GFX_TXN7
PCIE_RX8P AA32 / PCIE_RX8N Y32 ← GFX_TXP8 / GFX_TXN8
PCIE_RX9P Y31 / PCIE_RX9N W31 ← GFX_TXP9 / GFX_TXN9
PCIE_RX10P W30 / PCIE_RX10N V30 ← GFX_TXP10 / GFX_TXN10
PCIE_RX11P V32 / PCIE_RX11N U32 ← GFX_TXP11 / GFX_TXN11
PCIE_RX12P U31 / PCIE_RX12N T31 ← GFX_TXP12 / GFX_TXN12
PCIE_RX13P T30 / PCIE_RX13N R30 ← GFX_TXP13 / GFX_TXN13
PCIE_RX14P R32 / PCIE_RX14N P32 ← GFX_TXP14 / GFX_TXN14
PCIE_RX15P P31 / PCIE_RX15N N31 ← GFX_TXP15 / GFX_TXN15

PCIE_TX0P AK27 / PCIE_TX0N AJ27 → GFX_RXP0 / GFX_RXN0 (C3000 / C3001, E@0.1U_4)
PCIE_TX1P AJ25 / PCIE_TX1N AH25 → GFX_RXP1 / GFX_RXN1 (C3002 / C3003, E@0.1U_4)
PCIE_TX2P AH28 / PCIE_TX2N AG28 → GFX_RXP2 / GFX_RXN2 (C3004 / C3005, E@0.1U_4)
PCIE_TX3P AG27 / PCIE_TX3N AF27 → GFX_RXP3 / GFX_RXN3 (C3006 / C3007, E@0.1U_4)
PCIE_TX4P AF25 / PCIE_TX4N AE25 → GFX_RXP4 / GFX_RXN4 (C3008 / C3009, E@0.1U_4)
PCIE_TX5P AE28 / PCIE_TX5N AD28 → GFX_RXP5 / GFX_RXN5 (C3010 / C3011, E@0.1U_4)
PCIE_TX6P AD27 / PCIE_TX6N AC27 → GFX_RXP6 / GFX_RXN6 (C3015 / C3016, E@0.1U_4)
PCIE_TX7P AC25 / PCIE_TX7N AB25 → GFX_RXP7 / GFX_RXN7 (C3017 / C3018, E@0.1U_4)
PCIE_TX8P AB28 / PCIE_TX8N AA28 → GFX_RXP8 / GFX_RXN8 (C3022 / C3023, E@0.1U_4)
PCIE_TX9P AA27 / PCIE_TX9N Y27 → GFX_RXP9 / GFX_RXN9 (C3024 / C3025, E@0.1U_4)
PCIE_TX10P Y25 / PCIE_TX10N W25 → GFX_RXP10 / GFX_RXN10 (C3026 / C3027, E@0.1U_4)
PCIE_TX11P W28 / PCIE_TX11N V28 → GFX_RXP11 / GFX_RXN11 (C3028 / C3029, E@0.1U_4)
PCIE_TX12P V27 / PCIE_TX12N U27 → GFX_RXP12 / GFX_RXN12 (C3030 / C3031, E@0.1U_4)
PCIE_TX13P U25 / PCIE_TX13N T25 → GFX_RXP13 / GFX_RXN13 (C3032 / C3036, E@0.1U_4)
PCIE_TX14P T28 / PCIE_TX14N R28 → GFX_RXP14 / GFX_RXN14 (C3040 / C3037, E@0.1U_4)
PCIE_TX15P R27 / PCIE_TX15N P27 → GFX_RXP15 / GFX_RXN15 (C3042 / C3043, E@0.1U_4)

Clock
(2) CLK_PCIE_M56 → PCIE_REFCLKP AL28
(2) CLK_PCIE_M56# → PCIE_REFCLKN AK28
(14) M56_PLLTRST# → PERSTB AG24
PCIE_TEST AA24
PERSTB_MASK AF24
Tie To VSS
VCC3_M56 — R3024 E@10K_4 — AA24
R3022 E@10K_4 — AF24

Calibration
PCIE_CALRN AE24 — R3013 E@2K/F_4 — VCC1.2_VDDR
PCIE_CALRP AD24 — R3015 E@562
PCIE_CALI AB24 — R3019 E@1.47K

E@M56-P B26

CRT, DVI PU/PD
VCC3_M56
DVI_SCLK — R3035 E@4.7K_4
DVI_SDAT — R3036 E@4.7K_4
CRT_R — R3038 E@150/F_4
CRT_G — R3039 E@150/F_4
CRT_B — R3042 E@150/F_4

CRT2 PU
VCC3_M56
H2SYNC — R3030 *E@10K_4
V2SYNC — R3031 *E@10K_4
GENERICC — R3032 *E@10K_4

VCC3_M56 — R3005 *E@4.7K_4 / R3006 *E@4.7K_4
(7) LVDS_DATA
(7) LVDS_CLK
T3001 T3002 T3003 T3004 T3005 T3006

R3044 *E@10K_4 — GPIO4
(40) GPIO0 (40) GPIO1 (40) GPIO2 (40) GPIO3 (40) GPIO4 (40) GPIO5
T3008
LVDS_BLKEN
(40) GPIO8 (40) GPIO9
T3000
(40) GPIO11 (40) GPIO12 (40) GPIO13
R3016 E@10K_4
(33) V_PWRCNTL
(2) M56_27MHZ#
M56_ALERT#
R3021 E@499/F — R3023 E@499/F — VCC3_M56
M56_VREFG

M56_D+ AG12
M56_D- AH12
VCC2.5 — L3005 E@BLM18PG181SN1D_6 — +PVDD
C3047 E@10U/6.3V/X5R / C3048 E@0.1U_4 / C3049 E@1U/6.3V
M56_CORE
L3021 E@BLM18PG181SN1D_6
C3053 E@10U/6.3V/X5R / C3054 E@0.1U_4 / C3055 E@1U/6.3V
(2) M56_27MHZ — T3007
R3026 E@1K/F_4

GFX_TXP[15..0] → GFX_TXP[15..0] (7)
GFX_TXN[15..0] → GFX_TXN[15..0] (7)
GFX_RXP[15..0] → GFX_RXP[15..0] (7)
GFX_RXN[15..0] → GFX_RXN[15..0] (7)

M56 Thermal Sensor
C3056 E@2.2U/6.3V/X5R — R3000 E@200 — VCC3_M56
(3,40) KBSMCLK — KBSMCLK
(3,40) KBSMDATA — KBSMDATA
M56_ALERT# — ALERT
VCC3_M56 — R3126 E@10K_4 — T_CRIT_A
VCC3_M56 — R3029 E@10K_4
SMBCLK / SMDATA / ALERT / T_CRIT_A / VCC / D+ / D- / GND
M56_D+ — C3058 E@2200P — M56_D-
C3057 E@0.1U_4
U3000 E@LM89-1

GPIO_7_BLON PD
(7) LVDS_BLKEN — R3012 E@10K_4 — LVDS_BLKEN

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

U3001B

PART 2 OF 7

VIDEO & MULTIMEDIA

Expand GPIO
GPIO_34 GPIO_33 GPIO_32 GPIO_31 GPIO_30 GPIO_29 GPIO_28 GPIO_27 GPIO_26 GPIO_25 GPIO_24 GPIO_23 GPIO_22 GPIO_21 GPIO_20 GPIO_19 GPIO_18
(40) MEMTYP_1 (40) MEMTYP_0

NC_DVOVMODE_0 NC_DVOVMODE_1
DVPCNTL_0 DVPCNTL_1 DVPCNTL_2 DVPCLK
DVPDATA_0 DVPDATA_1 DVPDATA_2 DVPDATA_3 DVPDATA_4 DVPDATA_5 DVPDATA_6 DVPDATA_7 DVPDATA_8 DVPDATA_9 DVPDATA_10 DVPDATA_11 DVPDATA_12 DVPDATA_13 DVPDATA_14 DVPDATA_15 DVPDATA_16 DVPDATA_17 DVPDATA_18 DVPDATA_19 DVPDATA_20 DVPDATA_21 DVPDATA_22 DVPDATA_23
VIP Host/External TMDS

GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 GPIO_5 GPIO_6 GPIO_7_BLON GPIO_8 GPIO_9 GPIO_10 GPIO_11 GPIO_12 GPIO_13 GPIO_14 GPIO_15 GPIO_16 GPIO_17 NC_AB6
General Purpose I/O

VREFG
DPLUS DMINUS
Thermal Diode

PVDD PVSS MPVDD MPVSS XTALIN XTALOUT
PLL & XTAL

PLLTEST
TESTEN
Test
ROMCSb
ROM

LVSSR_1 LVSSR_2 LVSSR_3 LVSSR_4 LVSSR_5 LVSSR_6 LVSSR_7
LVDS PLL and I/O GND

External SSC
GENERICC
LPVSS
LVDS PLL and I/O GND
LVSSR_10 LVSSR_9 LVSSR_8

Integrated TMDS
TXCM AL9 / TXCP AM9 — R3001 E@180 — DVI_CLK# (25) / DVI_CLK (25)
TX0M AK10 / TX0P AL10 — R3002 E@180 — DVI_TX0# (25) / DVI_TX0 (25)
TX1M AL11 / TX1P AM11 — R3003 E@180 — DVI_TX1# (25) / DVI_TX1 (25)
TX2M AL12 / TX2P AM12 — R3004 E@180 — DVI_TX2# (25) / DVI_TX2 (25)
TX3M AK9 / TX3P AJ9
TX4M AK11 / TX4P AJ11
TX5M AK12 / TX5P AJ12

TPVDD AM8 — VCC25_M56_TPVDD — L3001 E@0_6 — VCC2.5 — max.20mA
C3012 E@0.1U_4 / C3013 E@1U/6.3V / C3014 E@10U/6.3V/X5R
TPVSS AL8
TXVDDR_1 AJ6 / TXVDDR_2 AK6 / TXVDDR_3 AL6 / TXVDDR_4 AM6 — VCC25_M56_TXVDDR — L3002 E@0_6 — VCC2.5 — max.200mA
C3019 E@10U/6.3V/X5R / C3020 E@0.1U_4 / C3021 E@0.1U_4
TXVSSR_1 AJ7 / TXVSSR_2 AK7 / TXVSSR_3 AL7 / TXVSSR_4 AM7 / TXVSSR_5 AK8

DAC / CRT
PLACE RGB TERMINATION RESISTORS CLOSE TO ASIC
R AK24 — CRT_R — CRT_R (7,11)
G AM24 — CRT_G — CRT_G (7,11)
B AL24 — CRT_B — CRT_B (7,11)
HSYNC AJ23 — HSYNC (7,11,25)
VSYNC AJ22 — VSYNC (7,11)
GENERICA AK22 — R3043 E@10K_4 — VCC3_M56
GENERICB AF23 — R3007 E@1K/F_4
RSET AL22 — R3008 E@499
AVDD_1 AL25 / AVDD_2 AM25 — VCC2.5_M56_AVDD — L3003 E@BLM18PG181SN1D_6 — VCC2.5 — max.65mA
C3033 E@1U/6.3V / C3034 E@0.1U_4 / C3035 E@10U/6.3V/X5R
AVSSQ AK23 / AVSSN_1 AK25 / AVSSN_2 AJ24
VDD1DI AM23 — VCC2.5_M56_VDDI — L3004 E@BLM18PG181SN1D_6 — VCC2.5 — max.20mA
C3038 E@1U/6.3V / C3039 E@0.1U_4 / C3041 E@10U/6.3V/X5R
VSS1DI AL23

DAC2 (TV/CRT2)
R2 AK15 / G2 AM15 / B2 AL15
H2SYNC AF15 — H2SYNC
V2SYNC AG15 — V2SYNC
PLACE RGB TERMINATION RESISTORS CLOSE TO ASIC
Y AJ15 — R3014 E@75
C AJ13 — R3017 E@75
COMP AH15 — R3018 E@75
R2SET AK14 — R3020 E@715/F
A2VDD_1 AM16 / A2VDD_2 AL16 — VCC2.5
C3045 *E@1U/6.3V / C3046 E@0.1U_4 / C3170 *E@22U/6.3V/X5R
A2VSSN_1 AM17 / A2VSSN_2 AL17
NC_A2VDDQ AL14 — M5x keep NC(M2x used)
A2VSSQ AK13
VDD2DI AJ16 — VCC2.5 — L3006 E@0_6
VSS2DI AJ17
C3051 *E@1U/6.3V / C3052 E@0.1U_4 / C3050 *E@22U/6.3V/X5R

Monitor Interface
HPD1 AF11 — DVI_HPD (25)
DDC1DATA AH22 — DDC2BD (7,11,25)
DDC1CLK AH23 — DDC2BC (7,11,25)
DDC2DATA AH13 — DVI_SDAT — DVI_SDAT (25)
DDC2CLK AG13 — DVI_SCLK — DVI_SCLK (25)
DDC3DATA AE12 — R3028 *E@0_4 — KBSMDATA
DDC3CLK AF12 — R3027 *E@0_4 — KBSMCLK
GENERICC AE23
LVSSR_10 AE18
LVSSR_9 AF22
LVSSR_8 AF17 / AF21

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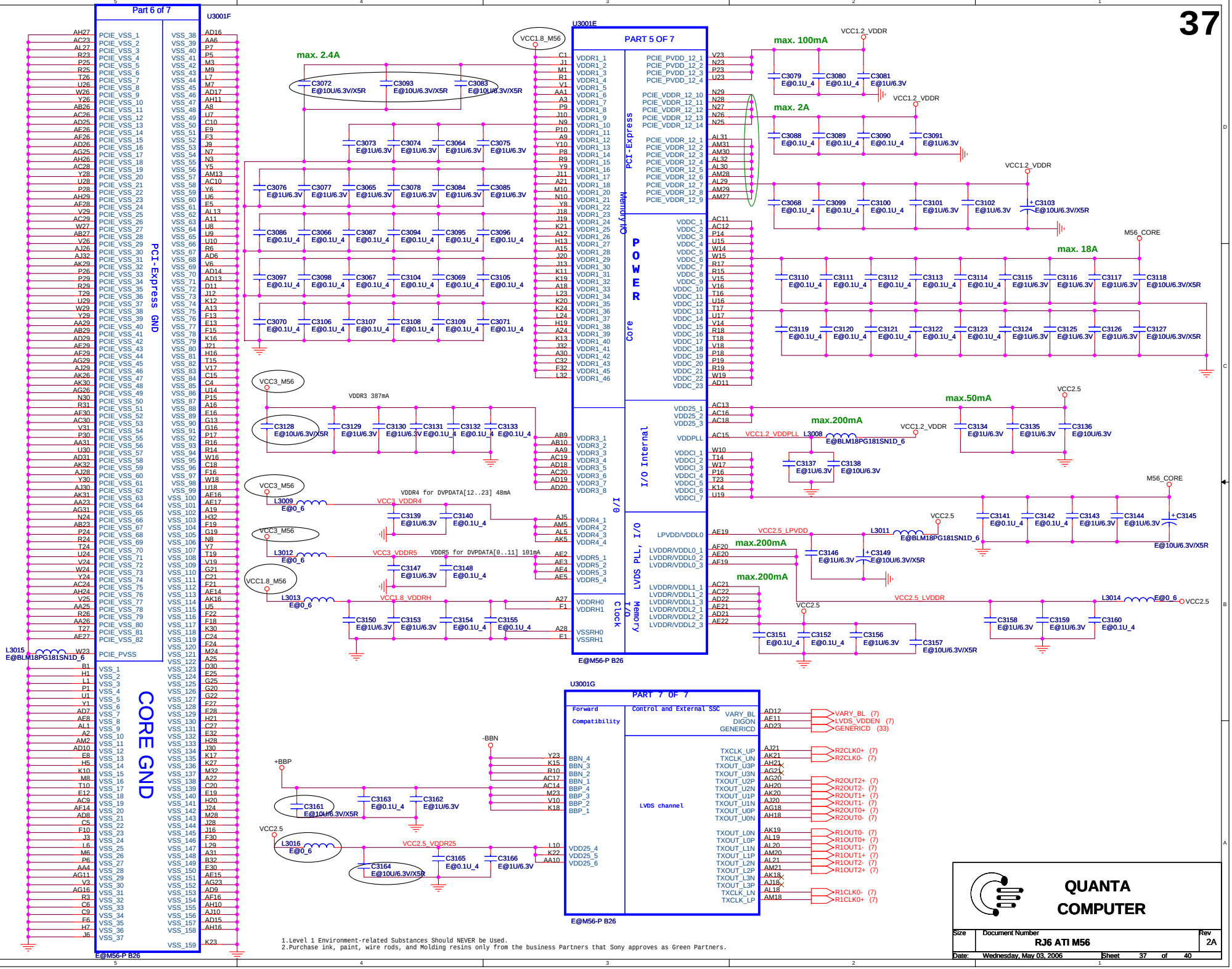
Part 6 of 7
U3001F
PCIE_VSS_1
PCIE_VSS_2
PCIE_VSS_3
PCIE_VSS_4
PCIE_VSS_5
PCIE_VSS_6
PCIE_VSS_7
PCIE_VSS_8
PCIE_VSS_9
PCIE_VSS_10
PCIE_VSS_11
PCIE_VSS_12
PCIE_VSS_13
PCIE_VSS_14
PCIE_VSS_15
PCIE_VSS_16
PCIE_VSS_17
PCIE_VSS_18
PCIE_VSS_19
PCIE_VSS_20
PCIE_VSS_21
PCIE_VSS_22
PCIE_VSS_23
PCIE_VSS_24
PCIE_VSS_25
PCIE_VSS_26
PCIE_VSS_27
PCIE_VSS_28
PCIE_VSS_29
PCIE_VSS_30
PCIE_VSS_31
PCIE_VSS_32
PCIE_VSS_33
PCIE_VSS_34
PCIE_VSS_35
PCIE_VSS_36
PCIE_VSS_37
PCIE_VSS_38
PCIE_VSS_39
PCIE_VSS_40
PCIE_VSS_41
PCIE_VSS_42
PCIE_VSS_43
PCIE_VSS_44
PCIE_VSS_45
PCIE_VSS_46
PCIE_VSS_47
PCIE_VSS_48
PCIE_VSS_49
PCIE_VSS_50
PCIE_VSS_51
PCIE_VSS_52
PCIE_VSS_53
PCIE_VSS_54
PCIE_VSS_55
PCIE_VSS_56
PCIE_VSS_57
PCIE_VSS_58
PCIE_VSS_59
PCIE_VSS_60
PCIE_VSS_61
PCIE_VSS_62
PCIE_VSS_63
PCIE_VSS_64
PCIE_VSS_65
PCIE_VSS_66
PCIE_VSS_67
PCIE_VSS_68
PCIE_VSS_69
PCIE_VSS_70
PCIE_VSS_71
PCIE_VSS_72
PCIE_VSS_73
PCIE_VSS_74
PCIE_VSS_75
PCIE_VSS_76
PCIE_VSS_77
PCIE_VSS_78
PCIE_VSS_79
PCIE_VSS_80
PCIE_VSS_81
PCIE_VSS_82
PCIE_PVSS
PCI-Express GND
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
VSS_6
VSS_7
VSS_8
VSS_9
VSS_10
VSS_11
VSS_12
VSS_13
VSS_14
VSS_15
VSS_16
VSS_17
VSS_18
VSS_19
VSS_20
VSS_21
VSS_22
VSS_23
VSS_24
VSS_25
VSS_26
VSS_27
VSS_28
VSS_29
VSS_30
VSS_31
VSS_32
VSS_33
VSS_34
VSS_35
VSS_36
VSS_37
CORE GND
E@M56-P B26
L3015
E@BLM18PG181SN1D_6
U3001E
PART 5 OF 7
PCI-Express
Memory I/O
POWER
Core
I/O Internal
I/O
LVDS PLL, I/O
Memory I/O
Clock
VDDR1_1
VDDR1_2
VDDR1_3
VDDR1_4
VDDR1_5
VDDR1_6
VDDR1_7
VDDR1_8
VDDR1_9
VDDR1_10
VDDR1_11
VDDR1_12
VDDR1_13
VDDR1_14
VDDR1_15
VDDR1_16
VDDR1_17
VDDR1_18
VDDR1_20
VDDR1_21
VDDR1_22
VDDR1_23
VDDR1_24
VDDR1_25
VDDR1_26
VDDR1_27
VDDR1_28
VDDR1_29
VDDR1_30
VDDR1_31
VDDR1_32
VDDR1_33
VDDR1_34
VDDR1_35
VDDR1_36
VDDR1_37
VDDR1_38
VDDR1_39
VDDR1_40
VDDR1_41
VDDR1_42
VDDR1_43
VDDR1_45
VDDR1_46
PCIE_PVDD_12_1
PCIE_PVDD_12_2
PCIE_PVDD_12_3
PCIE_PVDD_12_4
PCIE_VDDR_12_10
PCIE_VDDR_12_11
PCIE_VDDR_12_12
PCIE_VDDR_12_13
PCIE_VDDR_12_14
PCIE_VDDR_12_1
PCIE_VDDR_12_2
PCIE_VDDR_12_3
PCIE_VDDR_12_4
PCIE_VDDR_12_5
PCIE_VDDR_12_6
PCIE_VDDR_12_7
PCIE_VDDR_12_8
PCIE_VDDR_12_9
VDDC_1
VDDC_2
VDDC_3
VDDC_4
VDDC_5
VDDC_6
VDDC_7
VDDC_8
VDDC_9
VDDC_10
VDDC_11
VDDC_12
VDDC_13
VDDC_14
VDDC_15
VDDC_16
VDDC_17
VDDC_18
VDDC_19
VDDC_20
VDDC_21
VDDC_22
VDDC_23
VDD25_1
VDD25_2
VDD25_3
VDDPLL
VDDCI_1
VDDCI_2
VDDCI_3
VDDCI_4
VDDCI_5
VDDCI_6
VDDCI_7
VDDR3_1
VDDR3_2
VDDR3_3
VDDR3_4
VDDR3_5
VDDR3_6
VDDR3_7
VDDR3_8
VDDR4_1
VDDR4_2
VDDR4_3
VDDR4_4
VDDR5_1
VDDR5_2
VDDR5_3
VDDR5_4
LPVDD/VDDL0
LVDDR/VDDL0_1
LVDDR/VDDL0_2
LVDDR/VDDL0_3
LVDDR/VDDL1_1
LVDDR/VDDL1_2
LVDDR/VDDL1_3
LVDDR/VDDL2_1
LVDDR/VDDL2_2
LVDDR/VDDL2_3
VDDRH0
VDDRH1
VSSRH0
VSSRH1
E@M56-P B26
VCC1.8_M56
max. 2.4A
C3072 E@10U/6.3V/X5R
C3093 E@10U/6.3V/X5R
C3083 E@10U/6.3V/X5R
C3073 E@1U/6.3V
C3074 E@1U/6.3V
C3064 E@1U/6.3V
C3075 E@1U/6.3V
C3076 E@1U/6.3V
C3077 E@1U/6.3V
C3065 E@1U/6.3V
C3078 E@1U/6.3V
C3084 E@1U/6.3V
C3085 E@1U/6.3V
C3086 E@0.1U_4
C3066 E@0.1U_4
C3087 E@0.1U_4
C3094 E@0.1U_4
C3095 E@0.1U_4
C3096 E@0.1U_4
C3097 E@0.1U_4
C3098 E@0.1U_4
C3067 E@0.1U_4
C3104 E@0.1U_4
C3069 E@0.1U_4
C3105 E@0.1U_4
C3070 E@0.1U_4
C3106 E@0.1U_4
C3107 E@0.1U_4
C3108 E@0.1U_4
C3109 E@0.1U_4
C3071 E@0.1U_4
VCC3_M56
VDDR3 387mA
C3128 E@10U/6.3V/X5R
C3129 E@1U/6.3V
C3130 E@1U/6.3V
C3131 E@0.1U_4
C3132 E@0.1U_4
C3133 E@0.1U_4
VDDR4 for DVPDATA[12..23] 48mA
L3009 E@0_6
VCC3_VDDR4
C3139 E@1U/6.3V
C3140 E@0.1U_4
VCC3_M56
L3012 E@0_6
VCC3_VDDR5
VDDR5 for DVPDATA[0..11] 101mA
C3147 E@1U/6.3V
C3148 E@0.1U_4
VCC1.8_M56
L3013 E@0_6
VCC1.8_VDDRH
C3150 E@1U/6.3V
C3153 E@1U/6.3V
C3154 E@0.1U_4
C3155 E@0.1U_4
VCC1.8_M56
max. 100mA
C3079 E@0.1U_4
C3080 E@0.1U_4
C3081 E@1U/6.3V
max. 2A
C3088 E@0.1U_4
C3089 E@0.1U_4
C3090 E@0.1U_4
C3091 E@1U/6.3V
C3068 E@0.1U_4
C3099 E@0.1U_4
C3100 E@0.1U_4
C3101 E@1U/6.3V
C3102 E@1U/6.3V
C3103 E@10U/6.3V/X5R
M56_CORE
max. 18A
C3110 E@0.1U_4
C3111 E@0.1U_4
C3112 E@0.1U_4
C3113 E@0.1U_4
C3114 E@0.1U_4
C3115 E@1U/6.3V
C3116 E@1U/6.3V
C3117 E@1U/6.3V
C3118 E@10U/6.3V/X5R
C3119 E@0.1U_4
C3120 E@0.1U_4
C3121 E@0.1U_4
C3122 E@0.1U_4
C3123 E@0.1U_4
C3124 E@1U/6.3V
C3125 E@1U/6.3V
C3126 E@1U/6.3V
C3127 E@10U/6.3V/X5R
VCC2.5
max.50mA
max.200mA
VCC1.2_VDDPLL
L3008 E@BLM18PG181SN1D_6
C3137 E@1U/6.3V
C3138 E@10U/6.3V
C3134 E@1U/6.3V
C3135 E@1U/6.3V
C3136 E@10U/6.3V
M56_CORE
VCC2.5_LPVDD
L3011 E@BLM18PG181SN1D_6
C3146 E@1U/6.3V
C3149 E@10U/6.3V/X5R
C3141 E@0.1U_4
C3142 E@0.1U_4
C3143 E@1U/6.3V
C3144 E@1U/6.3V
C3145 E@10U/6.3V/X5R
max.200mA
max.200mA
VCC2.5_LVDDR
L3014 E@0_6
VCC2.5
C3151 E@0.1U_4
C3152 E@0.1U_4
C3156 E@1U/6.3V
C3157 E@10U/6.3V/X5R
C3158 E@1U/6.3V
C3159 E@1U/6.3V
C3160 E@0.1U_4
U3001G
PART 7 OF 7
Forward Compatibility
Control and External SSC
LVDS channel
VARY_BL
DIGON
GENERICD
TXCLK_UP
TXCLK_UN
TXOUT_U3P
TXOUT_U3N
TXOUT_U2P
TXOUT_U2N
TXOUT_U1P
TXOUT_U1N
TXOUT_U0P
TXOUT_U0N
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXCLK_LN
TXCLK_LP
VARY_BL (7)
LVDS_VDDEN (7)
GENERICD (33)
R2CLK0+ (7)
R2CLK0- (7)
R2OUT2+ (7)
R2OUT2- (7)
R2OUT1+ (7)
R2OUT1- (7)
R2OUT0+ (7)
R2OUT0- (7)
R1OUT0- (7)
R1OUT0+ (7)
R1OUT1- (7)
R1OUT1+ (7)
R1OUT2- (7)
R1OUT2+ (7)
R1CLK0- (7)
R1CLK0+ (7)
E@M56-P B26
-BBN
+BBP
C3161 E@10U/6.3V/X5R
C3163 E@0.1U_4
C3162 E@1U/6.3V
VCC2.5
L3016 E@0_6
VCC2.5_VDDR25
C3164 E@10U/6.3V/X5R
C3165 E@0.1U_4
C3166 E@1U/6.3V
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.
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Channel A

U3001C — Part 3 of 7 — MEMORY INTERFACE A

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For 8 Banks MAA_13=BA2

Use for DDR2 only, keep NC for others

Signal		DDR1,2	DDR3
MVREF to 1.8V		100R	40.2R
MVREF to GND		100R	100R

U3003 — E@VRAM_256Mb

U3004 — E@VRAM_256Mb

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Channel B

U3001D — Part 4 of 7 — MEMORY INTERFACE B

Signal		DDR1,2	GDDR3
MVREF to 1.8V		100R	40.2R
MVREF to GND		100R	100R

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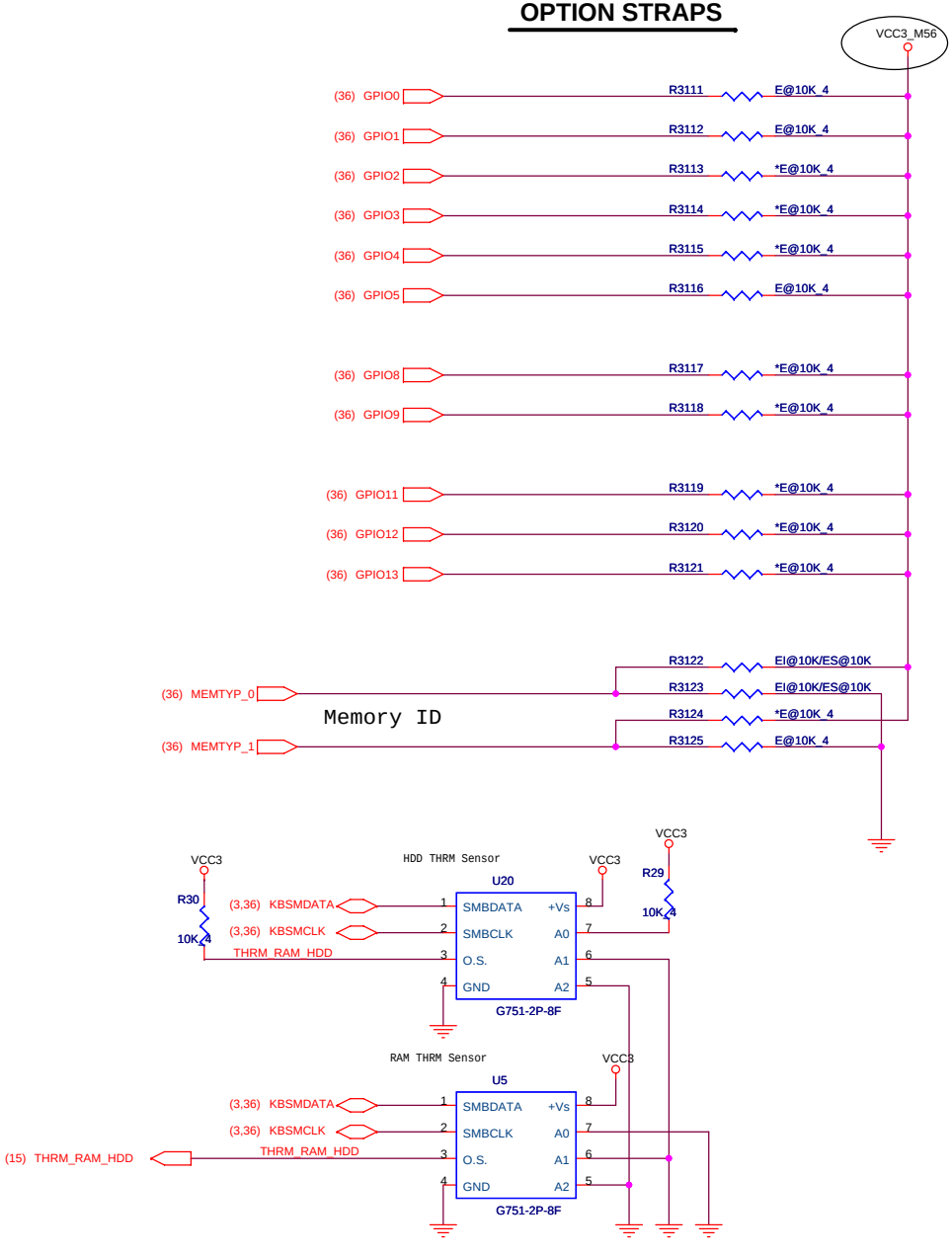
OPTION STRAPS



M56-P Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing (recommended)	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB(Default) 001x - No ROM,MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB 011x - No ROM,MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

VRAM Straps REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - TBD 11 - TBD	00

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